64000

HP64000
Logic Development
System

Service Manual

Model 64224S
80186
Emulator Subsystem

HEWLETT
PACKARD

CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

WARRANTY

This Hewlett-Packard system product is warranted against defects in materials and workmanship for a period of 90 days from date of installation. During the warranty period, HP will, at its options, either repair or replace products which prove to be defective.

Warranty service of this product will be performed at Buyer's facility at no charge within HP service travel areas. Outside HP service travel areas, warranty service will be performed at Buyer's facility only upon HP's prior agreement and Buyer shall pay HP's round trip travel expenses. In all other cases, products must be returned to a service facility designated by HP.

For products returned to HP for warranty service, Buyer shall prepay shipping charges to HP and HP shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to HP from another country.

HP warrants that its software and firmware designated by HP for use with an instrument will execute its programming instructions when properly installed on that instrument. HP does not warrant that the operation of the instrument, or software, or firmware will be uninterrupted or error free.

LIMITATION OF WARRANTY

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside the environmental specifications for the product, or improper site preparation or maintenance.

NO OTHER WARRANTY IS EXPRESSED OR IMPLIED. HP SPECIFICALLY DISCLAIMS THE IMPLIED WARRANTIES OF MERCHANTIBILITY AND FITNESS FOR A PARTICULAR PURPOSE.

EXCLUSIVE REMEDIES

THE REMEDIES PROVIDED HEREIN ARE BUYER'S SOLE AND EXCLUSIVE REMEDIES. HP SHALL NOT BE LIABLE FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER BASED ON CONTRACT, TORT, OR ANY OTHER LEGAL THEORY.

ASSISTANCE

Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.

For any assistance, contact your nearest Hewlett-Packard Sales and Service Office. Addresses are provided at the back of this manual.

HEWLETT
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64224S
80186 EMULATOR SUBSYSTEM

SERVICE MANUAL

REPAIR NUMBERS

This manual applies to components of the **64224S 80186 Emulator Subsystem** with the following repair number prefixes:

Model Number	Current Repair Prefix	Other Repair Prefixes
64223A	2416A	N/A
64224A	2417A	N/A

For further information on repair numbers refer to "Instruments Covered by This Manual" in Chapter 1.

SAFETY SUMMARY

The following general safety precautions must be observed during all phases of operation, service, and repair of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument. Hewlett-Packard Company assumes no liability for the customer's failure to comply with these requirements.

GROUND THE INSTRUMENT.

To minimize shock hazard, the instrument chassis and cabinet must be connected to an electrical ground. The instrument is equipped with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE.

Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS.

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with the power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE.

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY INSTRUMENT.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the instrument. Return the instrument to a Hewlett-Packard Sales and Service Office for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

> ## WARNING
>
> **Dangerous voltages, capable of causing death, are present in this instrument. Use extreme caution when handling, testing, and adjusting.**

SAFETY SYMBOLS

General Definitions of Safety Symbols Used on Equipment or in Manuals.

Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the instrument.

Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 volts must be so marked).

Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.

Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. A terminal marked with this symbol must be connected to ground in the manner described in the installation (operating) manual, and before operating the equipment.

Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.

Alternating current (power line).

Direct current (power line).

Alternating or direct current (power line).

The WARNING sign denotes a hazard. It calls attention to a procedure, practice, condition or the like, which, if not correctly performed, could result in injury or death to personnel.

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, condition or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product.

NOTE: The NOTE sign denotes important information. It calls attention to procedure, practice, condition or the like, which is essential to highlight.

Printing History

Each new edition of this manual incorporates all material updated since the previous edition. Manual change sheets are issued between editions, allowing you to correct or insert information in the current edition.

The part number changes only when each new edition is published. Minor corrections or additions may be made as the manual is reprinted between editions. Vertical bars in a page margin indicate the location of reprint corrections.

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Chapter 1
GENERAL INFORMATION

INTRODUCTION

This service manual contains information concerning the installation, maintenance, and troubleshooting for the Model 64224S 80186 Emulator Subsystem used as a component of the HP64000 Logic Development System. Troubleshooting theory contained in this manual allows the user to repair to the board level, which is supported under Hewlett-Packard's Bluestripe Exchange program.

Shown on the title page is a microfiche part number. This number can be used to order 4 X 6 inch microfilm transparencies of the manual. Each microfiche contains up to 96 photoduplicates of the manual pages.

SAFETY CONSIDERATIONS

This emulator has been designed and tested in accordance with IEC Publication 348, "Safety Requirements for Electronic Measuring Apparatus"; meets Hewlett-Packard Safety Class I; and has been shipped in a safe condition. The user should review both the manual and instrument for safety markings and safety instructions before operating the instrument. Of particular interest is the "Safety Summary", printed behind the title page of this manual. Additional items of interest are listed below.

Do Not Attempt to Disrupt Protective Ground

WARNING

Any interruption of the protective conductor inside or outside the apparatus or disconnection of the protective earth terminal is likely to make the apparatus dangerous. Intentional interruption of the protective conductor is prohibited.

Service and Maintenance - Qualified Personnel Only

Any adjustment, maintenance and repair of the opened instrument may only be carried out by qualified personnel aware of the hazards involved.

Do Not Use If Safety Features Have Been Impaired

If the safety features of the instrument have been damaged or defeated, the instrument shall not be used until repairs are effected which restore the safety features. The safety features of the instrument could be disabled in the following instances:

    a. The instrument shows visible damage.

    b. The instrument fails to perform correct measurements.

    c. The instrument has been shipped or stored under unfavorable environmental conditions. (Refer to Chapter 2 of this manual for information on environmental specifications of storage and shipment.)

MANUAL ORGANIZATION

This manual is organized into six chapters. Chapter 1 contains general information regarding manual applicability, instrument usage, instrument characteristics, and equipment requirements. Chapter 2 explains how to unpack and install the Model 64224S Emulator Subsystem; it also gives information on environmental limits for operating and non-operating conditions and packing instructions should the Emulator ever need to be shipped. Chapter 3 explains how to verify correct operation of the Model 64224S, and explains operation of the 80186 Emulator Subsystem. It also contains troubleshooting information should the Control Card fail the performance verification tests. Chapter 4 normally contains calibration information; however, there are no adjustments applicable to the 80186 Emulator Subsystem, so this chapter is blank. Chapter 5 explains how to order spare parts from Hewlett-Packard and lists the replacement parts which can be ordered for the Model 64224S. Chapter 6 is reserved for information corresponding to instrument changes which affect the manual.

INSTRUMENTS COVERED BY THIS MANUAL

Attached to the instrument or printed on the printed circuit board is the repair number. The repair number is in the form: 0000A00000. It is in two parts; the first four digits and the letter are the repair prefix, and the last five are the suffix. The prefix is the same for all identical instruments. The suffix, however, is assigned sequentially and is different for each instrument. The contents of this manual apply to instruments with the repair number prefix(es) listed on the title page.

An instrument manufactured after the printing of this manual may have a repair number prefix that is not listed on the title page. This unlisted repair number prefix indicates that the instrument is different from those described in this manual. The manual for this newer instrument is accompanied by a Manual Changes supplement. This supplement contains "change information" that explains how to adapt the manual for the newer instrument.

In addition to change information, the supplement contains information for correcting errors in the manual. To keep this manual as current as possible, Hewlett-Packard recommends that you periodically request the latest Manual Changes supplement. The supplement for this manual is identified with the manual print date and part number, both of which appear on the manual title page. Complimentary copies of the supplement are available from Hewlett-Packard.

For information concerning a repair number prefix that is not listed on the title page or in the Manual Changes supplement, contact your nearest Hewlett-Packard office.

DESCRIPTION

The Model 64224S is a component of the HP64000 Logic Development System. The development system is intended to aid engineers in the development of microprocessor based systems and peripherals. The system offers hardware and software emulation of selected microprocessors, along with high speed state and timing analysis, PROM programming, and software development in both assembly and high level languages.

The user may develop programs for the selected emulation processor using the editor, assembler/compiler, and relocatable linker utilities of the HP64000 system. This software may then be loaded into emulation or user memory prior to an emulation run, where it can be accessed at real-time speeds by the emulation processor.

Emulation means "to equal". As implemented in the HP64000 system, emulation allows the user to replace the processor in the system under development with a probe from the emulation within the HP64000 development system. The user can then run and analyze programs developed on the 64000 system while retaining all the features of the selected microprocessor.

The Model 64223A 8018X Emulator Control Card, when combined with the Model 64224A 80186 Emulator Pod, provides real time emulation of the Intel 80186 microprocessor. Features provided by the combination include single-stepping, real time program execution, and non-real time software analysis.

The 64224A 80186 Emulator Pod contains an 80186 microprocessor. The emulator may be used in a stand-alone mode (without a target system) for the purpose of developing, executing, and debugging software. It may then be inserted into the user's target system, allowing the debugged software to be run on the user's hardware.

EQUIPMENT REQUIRED

The 64223A 8018X Emulator Control Card must be connected to a 64224A 80186 Emulator pod, then installed in the HP64000 development station card cage. In addition, a 64155A Wide Address Memory Controller must be connected along with emulation memory boards providing a minimum of 8 kilobytes of RAM. This constitutes a minimum emulation subsystem. A 64302A Logic Analyzer is optional for providing real time analysis of software execution; a 64310A Software Performance Analyzer can provide real time analysis of software efficiency. Other logic analysis options are available. Please consult your HP Sales and Service office for possible configurations.

ELECTRICAL AND MECHANICAL CHARACTERISTICS

User Interface

The following lists the electrical and mechanical characteristics of the 80186 Emulator when installed in a user's target system:

>   Processor compatibility: compatible with Intel 80186 microprocessors and any other microprocessors that comply with the specifications of the Intel 80186.

>   Mechanical interface: to interface to the target system, the user must provide a socket complying with the specifications of either AMP 55162-X (socket) and AMP 55478-2 (lid) or IDT 3M Textool 268-5400-52.

>   Maximum clock speed: 8 MHz at the CLKOUT line; this corresponds to a maximum crystal frequency of 16 MHz.

>   Inputs/Outputs: one LSTTL load plus approximately 40 pF of shunt capacitance.

>   Target system power: approximately 25 mA of current is drawn from the target system's +5 V supply for in-circuit sensing; all other emulator power requirements are provided for by the development station.

Power Supply Requirements

The 64223A Emulator Control Card when combined with the 64224A Emulator Pod places the following demands on the 64000 development station power supply:

>   +5V -- 3.6 amperes typical (64223A/64224A combined).
>   All other supplies -- no power drawn by 64223A/64224A combination.

Chapter 2
INSTALLATION

INTRODUCTION

This section contains information necessary to install the Model 64224S 80186 Emulator Subsystem. Also included is information concerning initial inspection, damage claims, environmental considerations, storage, and shipment.

INITIAL INSPECTION

Inspect the shipping container for damage. If the shipping container or cushioning material is damaged, it should be kept until the contents have been checked for completeness and the 64224S has been checked mechanically and electrically. If the contents are incomplete, if there is mechanical damage or defect, or if the 64224S does not pass performance verification, notify the nearest Hewlett-Packard office. If the shipping container or cushioning material is damaged notify the carrier as well as the Hewlett-Packard office. The HP office will arrange for repair or replacement at HP option without waiting for claim settlement.

EMULATOR SUBSYSTEM INSTALLATION

The Model 64224A 80186 Emulator Pod must be connected to the Model 64223A 8018X Emulator Control Card before installation in the mainframe. Figures 2-1 and 2-2 are included to show the recommended placement of the Control Card in the 64000 mainframes. The preferred slot for the Emulator Control Card is the rearmost slot (if no analyzer is being used), or the second slot from the rear (if an analyzer is being used). This allows proper connection of cabling to the memory controller and optional analyzer; allows connection of the shielded pod cable assembly to the RFI ground bracket; and permits maximum free cable length outside the development station.

```
WARNING
```

READ THE SAFETY SUMMARY AT THE FRONT OF THIS MANUAL BEFORE INSTALLATION OR REMOVAL OF THE 64224S EMULATOR SUBSYSTEM.

64100 STATION FRONT

```
    ┌──────────────────────────┐
    │ ┌────────────────────┐   │
 A  │ │  _____  │   │      I/O BOARD
 B  │ │  _____  │   │      DISPLAY CONTROL BOARD
 C  │ │  _____  │   │      CPU BOARD
 0  │ │  _____  │   │      FLOPPY CONTROLLER BOARD
 1  │ │  _____  │   │      PROM PROGRAMMER
 2  │ │  _____  │   │      CONTROL BOARD MAY
 3  │ │  _____  │   │      BE IN ANY SLOT
 4  │ │  _____  │   │      (1 THROUGH 4)
 5  │ │  _____  │   │      EMULATOR MEMORY BOARD
 6  │ │  _____  │   │      EMULATOR MEMORY BOARD
 7  │ │  _____  │   │      WIDE MEMORY CONTROL BOARD
 8  │ │  _____  │   │      EMULATOR CONTROL BOARD
 9  │ │  _____  │   │      ANALYSIS BOARD
    │ └────────────────────┘   │
    └──────────────────────────┘
```

A. EMULATOR/ANALYSIS/MEMORY

64100 STATION FRONT

```
    ┌──────────────────────────┐
    │ ┌────────────────────┐   │
 A  │ │  _____  │   │      I/O BOARD
 B  │ │  _____  │   │      DISPLAY CONTROL BOARD
 C  │ │  _____  │   │      CPU BOARD
 0  │ │  _____  │   │      FLOPPY CONTROLLER BOARD
 1  │ │  _____  │   │      PROM PROGRAMMER
 2  │ │  _____  │   │      CONTROL BOARD MAY
 3  │ │  _____  │   │      BE IN ANY SLOT
 4  │ │  _____  │   │      (1 THROUGH 5)
 5  │ │  _____  │   │
 6  │ │  _____  │   │      EMULATOR MEMORY BOARD
 7  │ │  _____  │   │      EMULATOR MEMORY BOARD
 8  │ │  _____  │   │      WIDE MEMORY CONTROL BOARD
 9  │ │  _____  │   │      EMULATOR CONTROL BOARD
    │ └────────────────────┘   │
    └──────────────────────────┘
```

B. EMULATION/MEMORY

Figure 2-1. 64100A Card Cage Configuration

64110A STATION TOP

```
A  ————————
B  ————————
0  ————————
1  ————————
2  ————————
3  ————————
4  ————————
```

CPU/I–O BOARD
DISPLAY CONTROLLER
EMULATION MEMORY
EMULATION MEMORY
EMULATION MEMORY CONTROL
EMULATION CONTROL
ANALYSIS

A. EMULATOR/ANALYSIS/MEMORY

64110A STATION TOP

```
A  ————————
B  ————————
0  ————————
1  ————————
2  ————————
3  ————————
4  ————————
```

CPU/I–O BOARD
DISPLAY CONTROLLER
EMULATION MEMORY
EMULATION MEMORY
EMULATION MEMORY CONTROL
EMULATION CONTROL
BLANK

B. EMULATOR/MEMORY
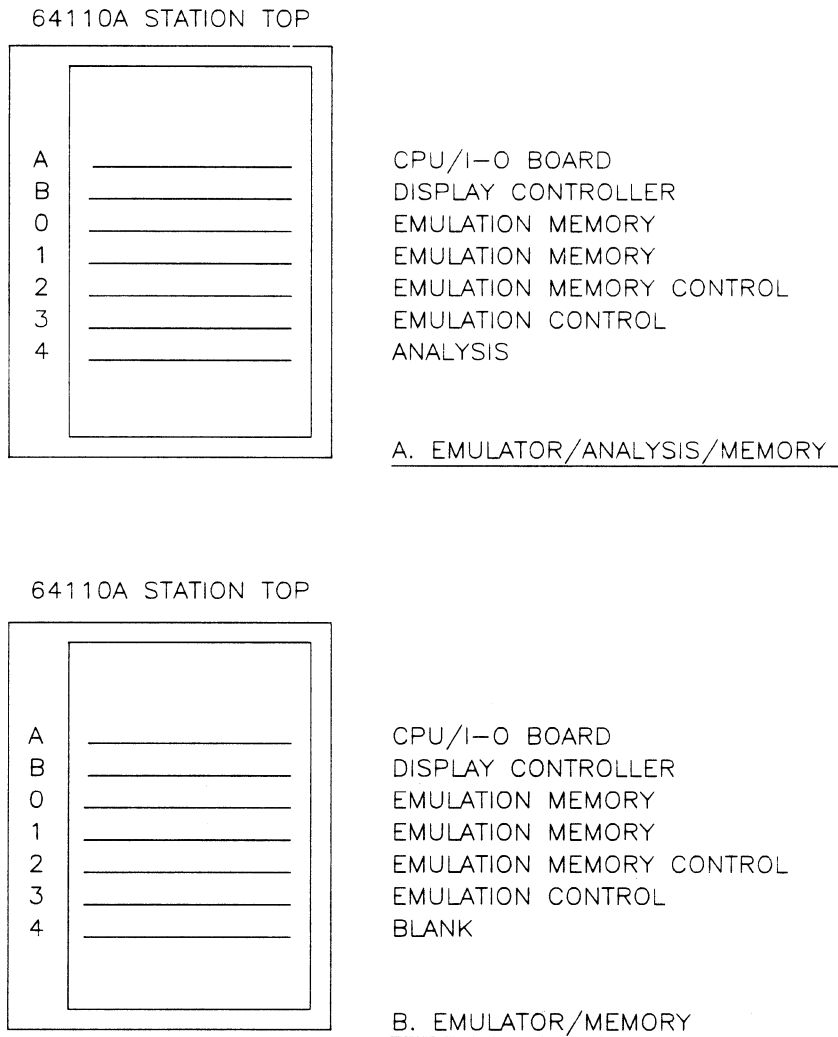
Figure 2-2. 64110A Card Cage Configuration

To install the 64224S, proceed as follows:

a. Turn off power to the 64000 development station.

```
~~~~~~~~~~~~~~
{ CAUTION }
~~~~~~~~~~~~~~
```

Power to the 64000 development station must be removed before
installation or removal of option cards (emulation, etc.) to avoid
damage to the option cards and the development station.

b. Loosen the two hold-down screws and remove the card cage access cover (64100A).
(Refer to the 64110A Mainframe Service Manual for information on removing the card cage
access cover of a 64110A.)

c. If you are installing the 64224S in a 64100A development station, verify that the RFI
Ground Bracket (A4MP7; shown in figure 2-11) has been installed in the mainframe as
shown in figure 2-12. If it has not, go to the paragraph entitled "RFI Ground Bracket
Installation" in this section to install the bracket. After installation, proceed with step d.

d. The emulation memory controller bus cables each have a 50 pin card edge connector on
one end and a 50 pin block connector on the other end. The block connectors are to be
connected to the matching block connectors at the middle center and right center of the
emulation control card. See figure 2-3. Align pin 1 of the male and female connector sets
and join the two block connectors for each cable.

e. Now the Emulator Pod is to be connected to the Emulator Control Card. (Refer to figure
2-3.) Two multi-colored ribbon cables within a shield braid assembly are used to connect the
pod to the card. One cable is terminated in a female card-edge connector; the other is
terminated in a female socket type connector. Pin 1 of each connector is indicated by a
triangle molded into the connector. The mating male connectors are at the top left corner of
the Control Card (as you face the component side of the board). Pin 1 of the card edge
connector is indicated by a "1" etched on the board surface; Pin 1 of the block connector is
indicated by a triangle molded into the connector block. Note that the block connector on
the board is a latching type. Verify that the connector is open (latching tips spread towards
the outside edges of the board) before installing the emulator pod cables. Making sure to
align pin 1 of the male and female connectors, connect the pod to the control board by
joining the two connector sets. When installing the block connector, push down on the
female connector until the latching tips snap over the top of the connector.
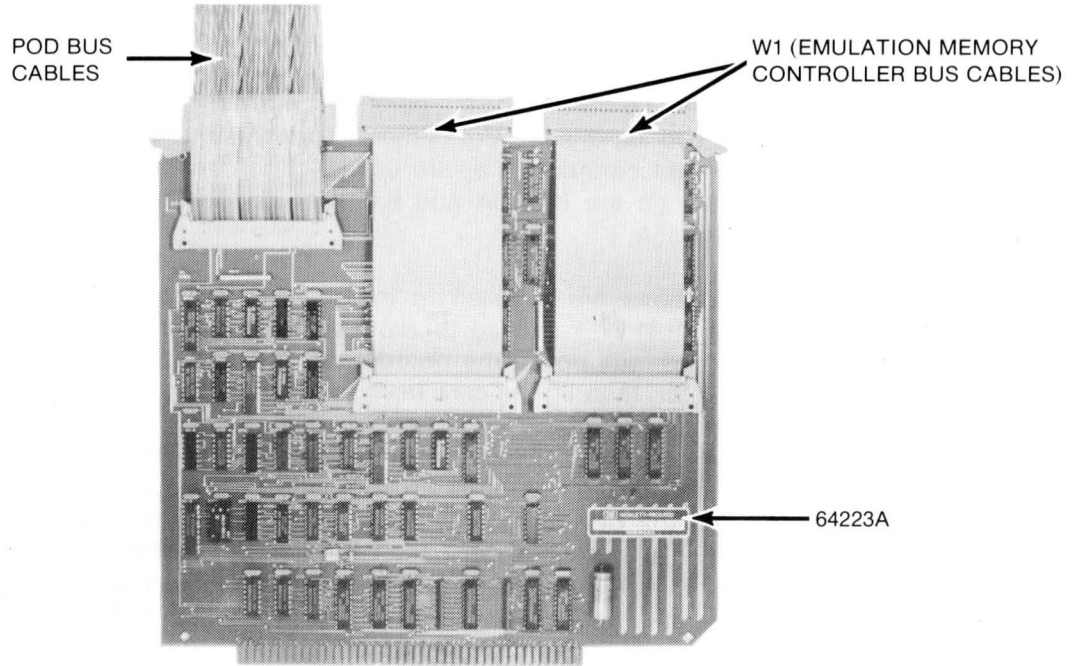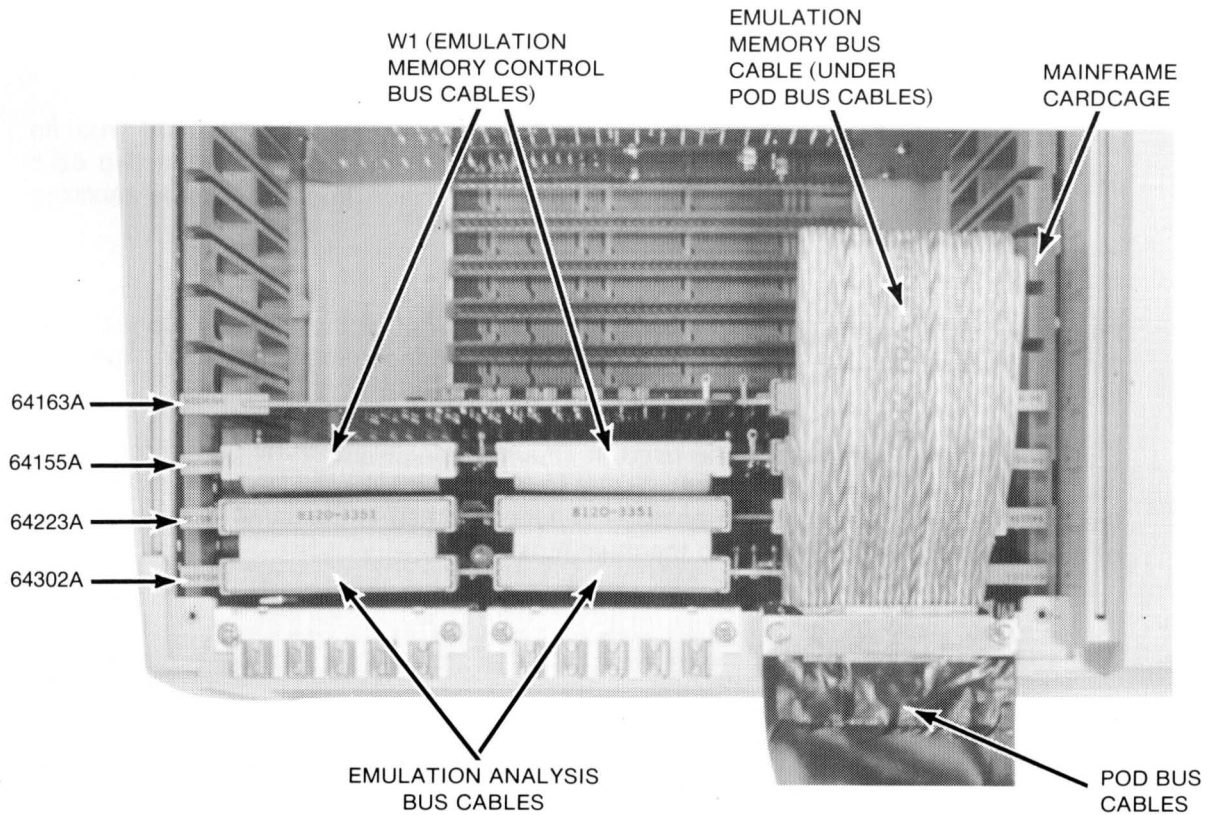
Figure 2-3. Memory Control Bus Cable Connection

Figure 2-4. Emulation Bus Cable Connections

f. To ease installation of the 64223A Emulator Control Card, the Control Card should be connected to the 64155A memory controller before installation of either into the card cage. First, lay the 64223A Emulator Control Card on a flat surface with the component side up, the large connector (P1) pointing towards you, and all the attached cables laying flat against the board and pointing away from you. Then lay the 64155A Wide Memory Controller board on top of the 64223A with connector P1 pointing towards you and the component side up. Next, connect the two card edge connectors from the memory controller cables on the 64223A to the top right connectors of the 64155A; the center connector on the 64223A to the center connector on the 64155A and the right connector on the 64223A to the right connector on the 64155A.

g. Verify that no options are installed in the rear of the card cage. If any options are installed here, they must be removed to allow easy installation of the 80186 emulator. To remove an option card, pull up on the board extractor tabs until the card snaps free of the motherboard connector, then lift the card from the cardcage.

h. Now the 64223A Control Card and the 64155A memory controller must be installed in the card cage. To do this, grasp the cards at each side with the component side of the cards towards the front of the development station and the card edge connectors labeled "P1" towards the bottom of the card cage. Insert the cards into the guide rails of the selected slots (refer to figure 2-1 or 2-2). For example, if you are installing the emulator in a 64100A development station and will be using an analyzer in slot #9, then the 64223A card should be inserted in the guide rails of slot #8 and the 64155A card should be inserted in the guide rails of slot #7. Making sure the connectors "P1" and the edge connector sockets on the Motherboard are aligned, push the cards down until each seats firmly in its respective socket.

NOTE

It will be easier to insert the cards if you push the 64155A card into its motherboard socket first after aligning both cards within their respective card cage guide rails. This is due to a length limitation imposed by the memory controller cables from the 64223A to the 64155A.

Follow by installing the required memory boards in front of the Memory Controller (refer to the applicable service manual for instructions concerning emulation memory card installation).

i. If an optional analyzer is to be used, it should be installed in the slot immediately to the rear of the Emulator Control Card. (Refer to the applicable service manual while installing the analyzer.) Installation of the analyzer is accomplished in the same manner as installation of the Emulator Control Card into the mainframe.

j. The emulation bus and emulation memory bus cables should be installed at this point. A list of available emulation bus cables and their corresponding HP part numbers is provided below.

Table 2-1. Emulation Bus Cables

```
Cable                 HP Part Number

Two Connector         8120-3351
Three Connector       8120-3352
Four Connector        8120-3353
Five Connector        8120-3345
```

Figure 2-4 shows where the cables should be installed when a complete emulation subsystem is installed - emulator, emulation memory control and emulation memory, and analysis.

k. The ground bar clamp must now be attached to the emulator pod cable shielding and to the mainframe to provide RFI suppression. Refer to Figure 2-11 for an illustration of the clamp (A4MP1); refer to either figure 2-12 (64100A) or figure 2-13 (64110A) as appropriate for details concerning clamp installation while following the procedure given below.

64100A

1. The emulator pod cable shield braid has two perforations. Place the perforation nearest the RFI ground bracket stud over the stud and press down gently until the cable lays flat across the top rear of the mainframe.

2. Place the single hole end (NOT the slot end) of the ground bar clamp (A4MP1) over the RFI ground bracket stud in such a manner that the open end of the slot points in a clockwise direction as viewed from the top of the development station. Thread a single nut (A4MP5) onto the stud. Do not tighten the nut at this point.

3. Insert the long screw (A4MP4; depicted in figure 2-11) into the slot end of the ground bar clamp. Continue by inserting the screw through the free end of the ground shield braid and on into the RFI ground bracket. Attach a nut (A4MP5) to the free end of the screw (inside the top cover of the development station at this point) and tighten firmly enough to hold the bar clamp in place but not so tight as to damage the emulator pod cables.

4. Tighten the nut placed on the stud in Step 2, being sure to observe the cautions given in Step 3.

5. Up to two sets of emulator pod cables can be grounded in this fashion, using the procedure described above.

64110A

1. Insert a screw (A4MP2) through the single hole end (NOT the slot end) of the ground bar clamp (A4MP1). Continue with the screw through the right most perforation of the emulator pod cable shield braid and the right most hole of the sheet metal in the rear of the mainframe. (Right most as viewed from the rear of the mainframe. Refer to figure 2-14 for details.)

2. Repeat the procedure with another screw; this time, use the slot end of the bar clamp and the holes in the shield braid and sheet metal immediately left of the right most position (refer to figure 2-14).

l. Reinstall the card cage access cover and tighten the 2 screws (64100A). (Refer to the 64110A Mainframe Service Manual for information on replacing the card cage access cover of the 64110A.)

EMULATOR REMOVAL

To remove the 64224S use the following procedure:

WARNING

READ THE SAFETY SUMMARY AT THE FRONT OF THIS MANUAL BEFORE INSTALLATION OR REMOVAL OF THE 64224S EMULATOR SUBSYSTEM.

a. Turn off power to the 64000 development station.

CAUTION

Power to the 64000 development station must be removed before installation or removal of option cards (emulation, etc.) to avoid damage to the option cards and the development station.

b. Remove the card cage access cover.

c. Disconnect the emulator pod from the target system and from the emulator control card, if you have not already done so.

c. Remove the emulation bus cables.

d. Remove the RFI ground bar clamp.

e. Disconnect the emulation memory bus cable from the 64223A to the 64155A.

f. Pull up on the board extractor levers of the 64223A and lift the card clear of the development station card cage.

EMULATOR POD DISASSEMBLY

To disassemble the Model 64224A 80186 Emulator Pod for troubleshooting and repair, use the following procedure:

a. Remove the emulator from the mainframe, using the procedure described earlier.

b. Unplug the two user enhancement cable assemblies from the end of the emulator pod. (These can be removed by grasping the cable at the point where it enters the emulator pod and pulling firmly away from the pod.)

c. Remove the three screws on each side of the emulator pod (MP7, see figure 2-5).

d. Remove the four screws from the top cover of the emulator pod (MP7, see figure 2-6).

e. Turn over the emulator pod and remove the two screws (MP5) at each end of the pod which are nearest the rubber bumper feet. Refer to figure 2-7.

f. Carefully pull the emulator pod's top cover away from its bottom cover, making sure to unplug the user enhancement cable (W3; figure 2-8) from the board nearest the top cover as you do so.

g. Further disassembly of the pod top cover may be accomplished by removing the two screws (MP5; figure 2-8) which hold each endcap to the sheet metal.

h. The metal RFI shields are removed from the pod bottom cover by removing the two screws securing each shield to the cover (MP5, see figure 2-7). (Note: do not remove these screws unless it is absolutely necessary to fully disassemble the pod.)

i. Remove the emulator PC boards (A1 & A2) by removing the 7 screws securing the board spacers to the pod bottom cover (MP6, see figure 2-7).

j. To disconnect the pod bus cable (W2, see figure 2-9) pull outward on the latching tips of the connectors which hold the multi-colored ribbon cables to the pod boards. See figure 2-9. The female block connectors terminating the ends of the ribbon cables should snap free.

k. To disconnect the emulator pod boards from each other, pull outwards on the latching tips of the connectors on the A2 board which hold the ribbon cables from the A1 board. See figure 2-9.

l. To remove the user cable (W1) from the emulator pod A1 board, unscrew the two screws (MP3) which hold the ribbon cable clamp halves (MP8, MP9; one on each side of the A1 board) together. See figure 2-10. Grasp each female block connector of the user cable one at a time and pull it away from the matching male block connector. (There are four such connections.)

MP7 (SCREWS)

MP10
(TOP COVER)

A3 (BOTTOM COVER)
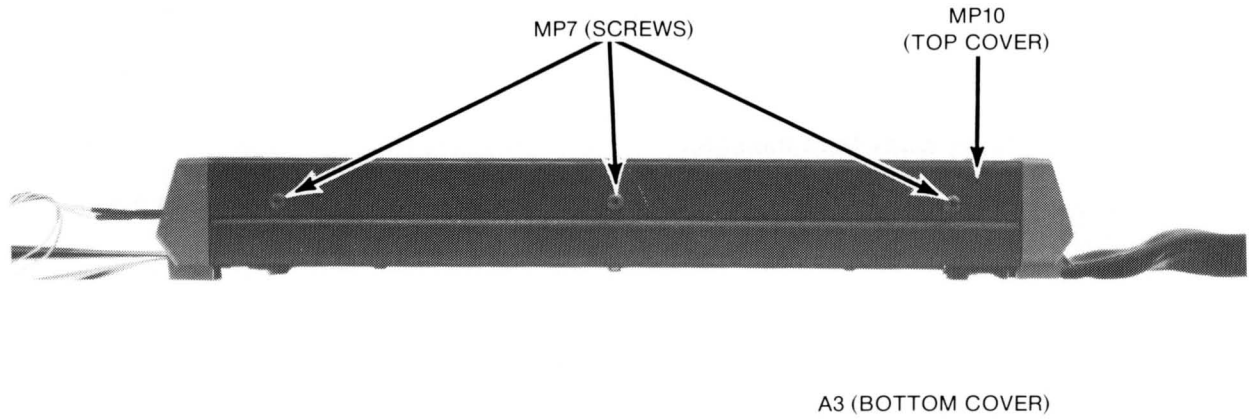
Figure 2-5. 80186 Emulator Pod Side View
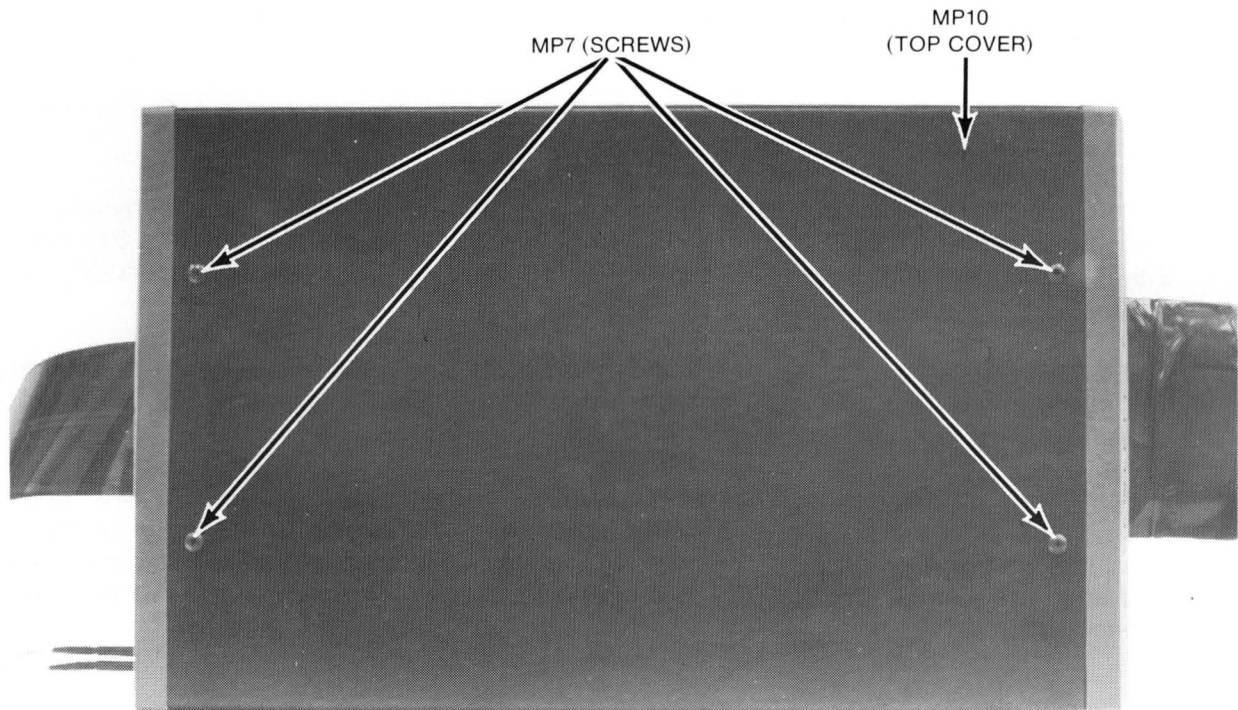
MP10
(TOP COVER)

MP7 (SCREWS)
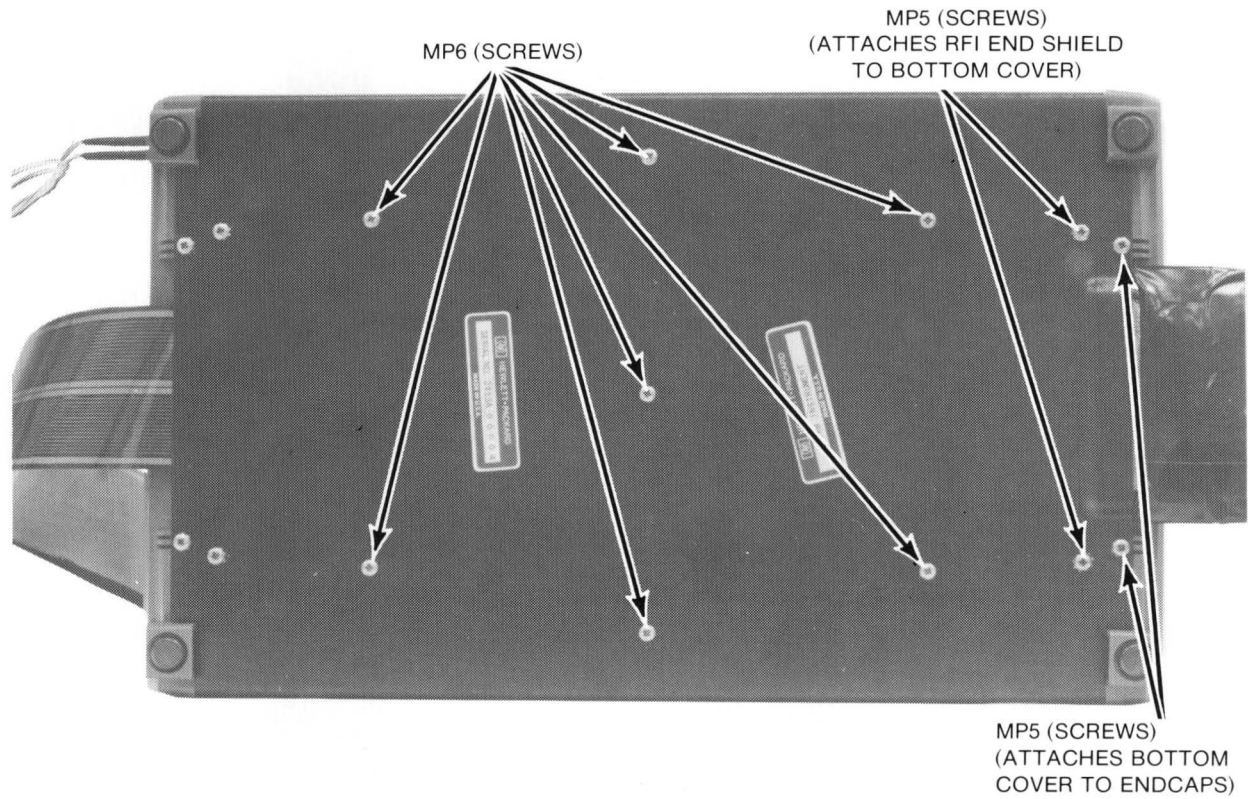
Figure 2-6. 80186 Emulator Pod Top View

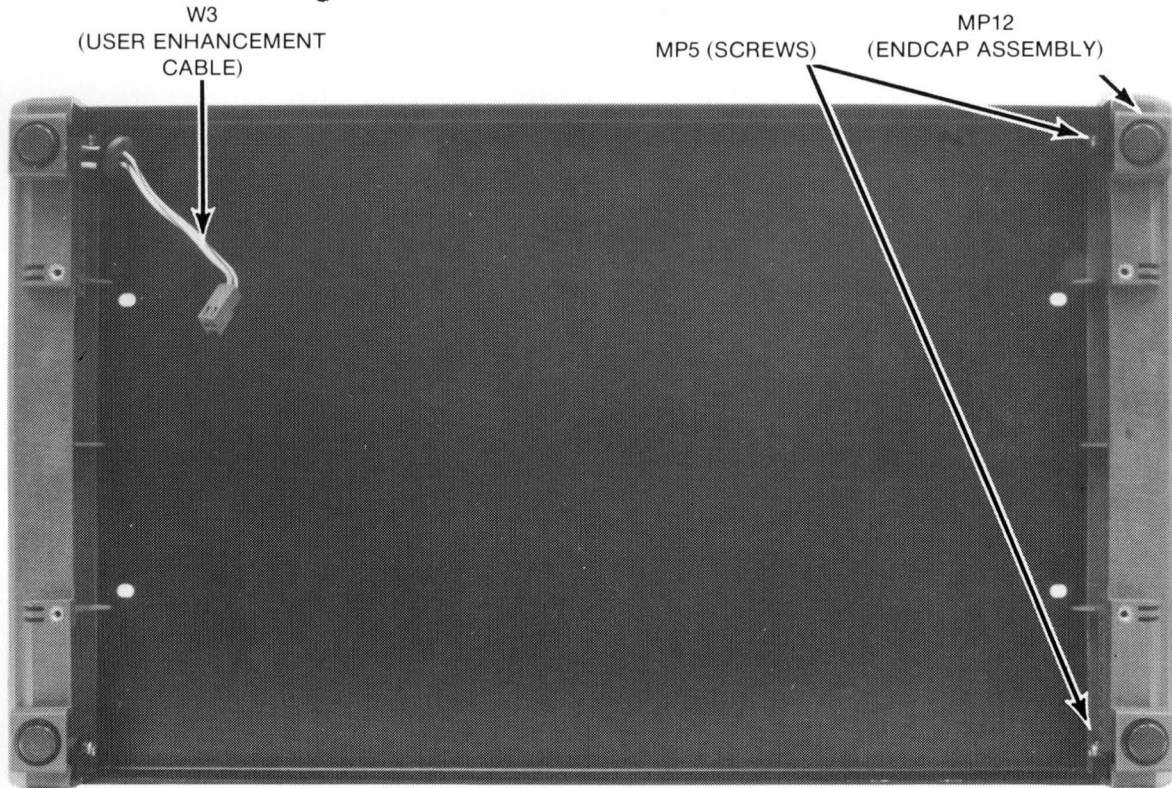Figure 2-7. 80186 Emulator Pod Bottom View
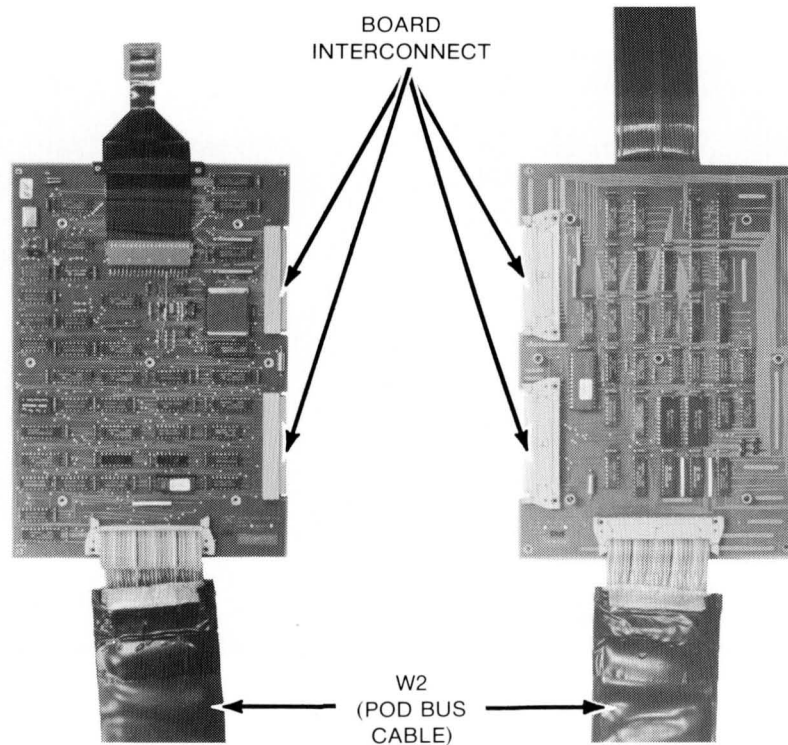

Figure 2-8. Emulator Pod - Inside Top Cover

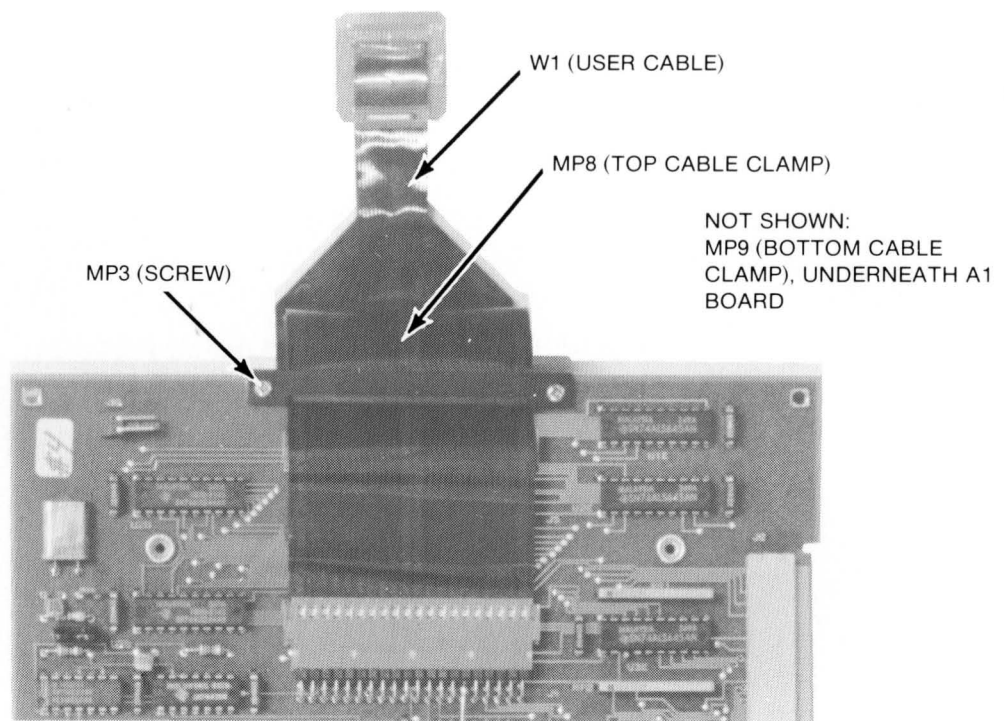Figure 2-9. Pod Bus and Board Interconnect Cables

Figure 2-10. User Cable and Cable Clamp Attachment

EMULATOR POD REASSEMBLY

To reassemble the emulator pod, proceed as follows:

a. To connect the user cable (W1) to the emulator pod A1 microprocessor board, proceed as follows:

1. Lay the pod A1 board down on a flat surface with the component side up. (See figure 2-10.) Orient the user cable so that the two short ends of the cable are underneath the long ends and pointing towards the A1 board with the user probe connector pointing away from the board. The short user cable ends should be connected to the male pin connectors nearest one end of the board with the bottom most cable end connected to the bottom male pin connector.

2. Now connect the long cable ends of the user cable to the male pin connector near the center of the board. The bottom most long cable end should be connected to the pin connector nearest the board surface.

b. Replace the cable clamp by putting the bottom half of the clamp (MP9; threaded sockets) on the circuit side of the A1 board with the protruding side of the clamp pointing away from the circuit board and away from the outside edge of the board. The top half of the clamp (MP8; no threads) should be placed over the user cable on the component side of the board; orientation is the same as for the bottom half. See figure 2-10 for details. Use the two short 2-56 screws (MP3, figure 2-10) to screw together the top and bottom halves of the clamp; be sure not to overtighten the screws, as this would damage the flex cable.

c. Reconnect the A1 board and A2 board by joining the female block connectors from the A1 board interconnect cables to the male pin connectors on the A2 board. See figure 2-9. Make sure that the latching tips of the connectors are open before joining the connectors, then press the two connector sets together until the latching tips snap over the top of the cable connectors.

Fold the cables over so that the component side of one board is facing in the opposite direction of the component side of the other board.

d. Connect the pod bus cables (W2; see figure 2-9) to the emulator pod circuit boards. Each multi-colored ribbon cable can only connect to one of the matching connectors at the end of each pod board.

e. Reattach the pod boards to the bottom cover by placing the folded board set inside the bottom cover and inserting the 7 screws (MP6; figure 2-7) from the outside of the cover. The A2 board should be closest to the bottom cover and the user cable should pass over the end of the bottom cover which has the protective rubber trim strip (A3MP1).

f. Replace the RFI end shields. One of these attaches to each end of the pod bottom cover with the slotted end pointing away from the bottom cover (this provides egress for the user enhancement cables) and the standoff end towards the bottom cover (the standoffs provide room for the user cable and pod bus cable to be sandwiched in between the shield and the bottom cover). Do not overtighten the screws attaching the end shields to the bottom cover; to do so might damage the cables.

g. If the emulator pod endcaps were removed from the top cover, reattach them using screws MP5; refer to figure 2-8 for details.

h. Reattach the pod top cover to the bottom cover as follows:

1. Reconnect the user enhancement cable (W3) from inside the top cover to the 2 pin connector on the pod A1 board assembly.

2. Seat the grommet (MP1) from the cable into the RFI end shield notch near one end of the shield.

3. Place the pod top cover over the pod bottom cover; insert and tighten the four screws (MP5; figure 2-7) nearest the pod bumper feet.

4. Insert and tighten the four screws (MP7; figure 2-6) which attach the RFI end shields to the pod top cover.

5. Insert and tighten the six screws (MP7; figure 2-5) which hold each side of the pod top cover to the pod bottom cover.

A4 ASSEMBLY

A4MP7

A4MP1

A4MP4   A4MP3   A4MP2   A4MP5
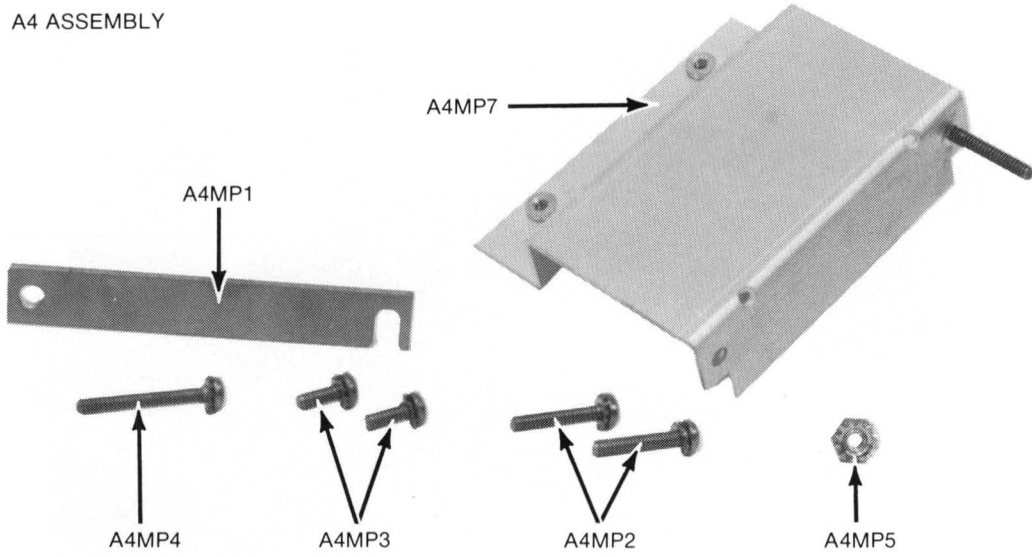
Figure 2-11. RFI Ground Bracket Assembly Parts
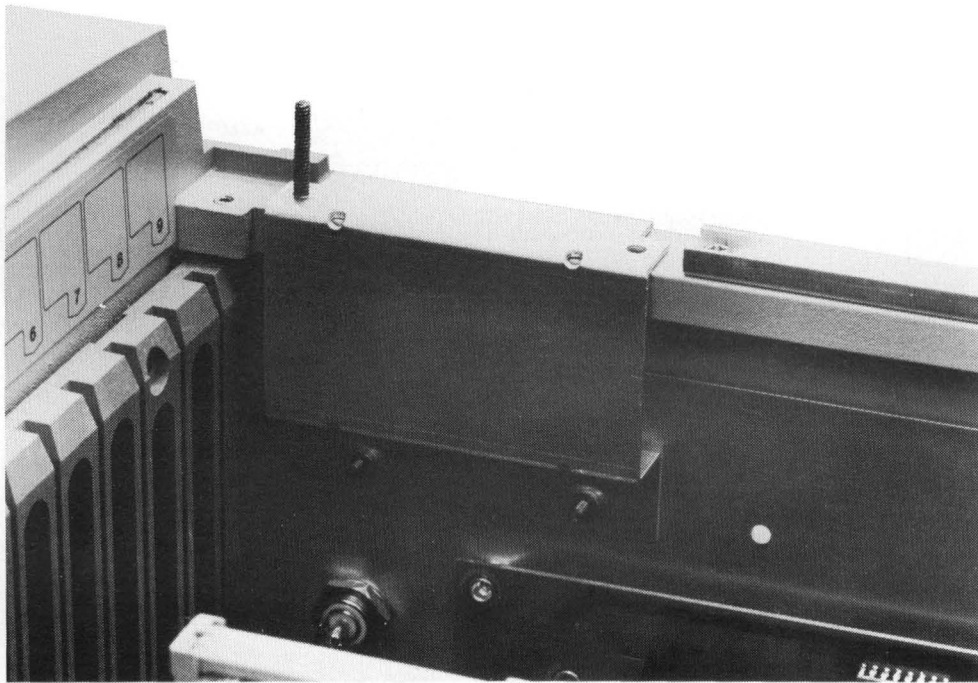
Figure 2-12. RFI Ground Bracket Installation (64100A)

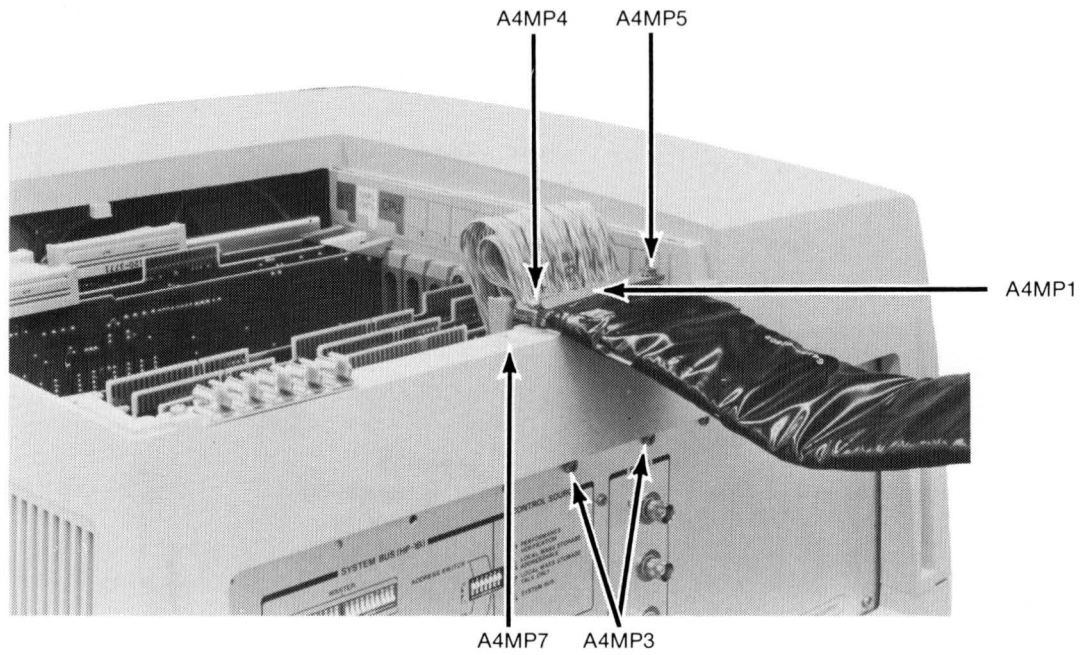A4MP4   A4MP5

A4MP1

A4MP7   A4MP3

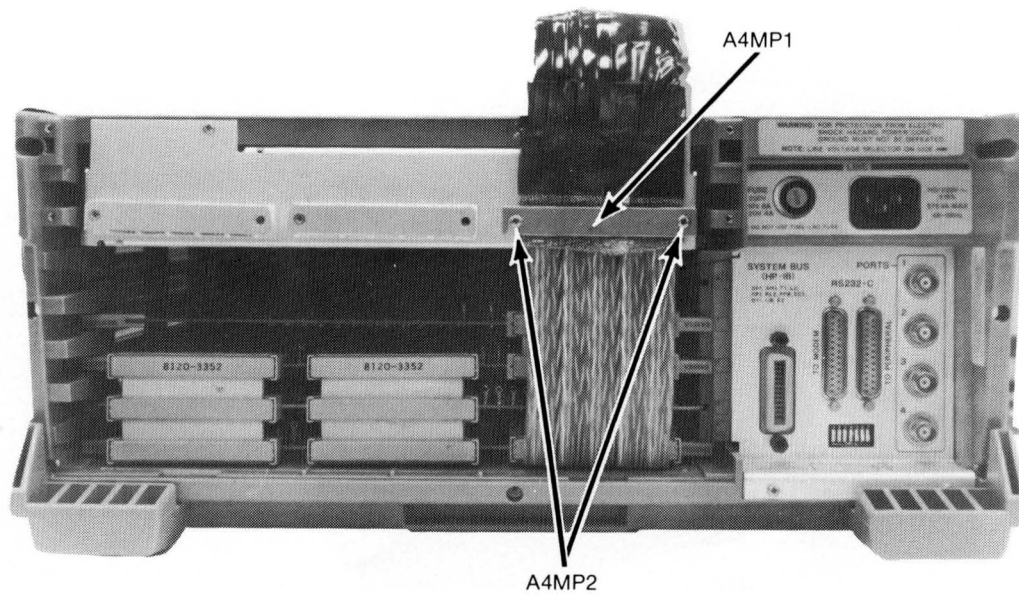Figure 2-13. Ground Bar Clamp Installation (64100A)

A4MP1

A4MP2

Figure 2-14. Ground Bar Clamp Installation (64110A)

RFI GROUND BRACKET INSTALLATION

An RFI Ground Bracket must be installed in the 64100A mainframe before installing the 64223A Emulator Control Card and the 64224A Emulator Pod. The purpose of this ground bracket is to connect the emulator pod cable shield braid to earth ground. This effectively prevents the emission of radio frequency interference components from the pod cables.

No ground bracket is required on the 64110A development station, since the bar clamp holding the shield braid to the mainframe bolts into existing sheet metal which is at ground potential.

The RFI ground bracket parts are included with the 64224A 80186 Emulator Pod. For convenience, a photograph depicting all the parts is reproduced here; table 2-2 gives a short listing of the parts included in the ground bracket assembly (A4 for the 80186 Emulator Pod).

Table 2-2. RFI Ground Bracket Assembly Parts

REF DES	DESCRIPTION	PART #
A4	GROUND BRACKET ASSY	64100-62102
A4MP1	GROUND BAR CLAMP	1531-0273
A4MP2	SCREW 4-40 3/4"	2200-0151
A4MP3	SCREW 6-32 3/8"	2360-0117
A4MP4	SCREW 6-32 1"	2360-0129
A4MP5	NUT 6-32	2420-0001
A4MP6	WASHER	3050-0235
A4MP7	RFI GROUND BRACKET	64100-01205

To install the ground bracket on the 64100A development station, proceed as follows:

WARNING

READ THE SAFETY SUMMARY AT THE FRONT OF THIS MANUAL BEFORE INSTALLATION OR REMOVAL OF THE 64224S EMULATOR SUBSYSTEM.

a. Turn off power to the 64000 development station and remove the card cage access cover.

CAUTION

Power to the 64000 development station must be removed before installation or removal of option cards (emulation, etc.) to avoid damage to the option cards and the development station.

a. If no ground bracket is installed in the mainframe, then the old U-shaped bracket on the rightmost side of the mainframe top cover (as viewed from the rear) must be removed. Loosen the two screws; remove the bracket; discard the bracket and the screws (they will not be needed for the RFI bracket).

b. Place the RFI bracket on the top rear cover of the mainframe in the rightmost cable position (as viewed from the rear of the station) with the threaded stud on the bracket pointing upwards and the U-shaped portion of the bracket to the inside of the card cage. Refer to figure 2-12 for details.

c. Refer to figure 2-13. Thread two screws (A4MP3) into the RFI bracket from the outside of the development station rear panel sheet metal. Tighten the screws firmly.

d. To remove the bracket, reverse the installation procedure.

OPERATING ENVIRONMENT

The 64224S may be operated in environments within the following limits:

Temperature. . . . .0° to +40° C
Humidity. . . . . 5% to 80% relative humidity
Altitude. . . . . 4 600 m (15 000 ft)

It should be protected from temperature extremes which could cause condensation within the instrument.

STORAGE AND SHIPMENT

Environment

The 64224S may be stored or shipped in environments within the following limits:

Temperature. . . . . -40° to +75° C
Humidity. . . . . 5% to 80% relative humidity
Altitude. . . . . 15 000 m (50 000 ft)

Original Packaging

Containers and packing materials identical to those used in factory packaging are available through Hewlett-Packard offices.

Other Packaging

The following general instructions should be used for re-packing with commercially available materials:

a. Wrap the emulator component (64223A or 64224A) in heavy paper or plastic.

b. Use a strong shipping container. A double-wall carton made of 350-pound test material is adequate.

c. Use a layer of shock-absorbing material 70 to 100 mm (3 to 4 inches) thick around all sides of the components to provide firm cushioning and prevent movement inside the container.

d. Seal shipping container securely.

e. Mark shipping container FRAGILE to ensure careful handling.

f. In any correspondence, refer to instrument by model number and full serial number.

CAUTION

The following precautions should be taken while using Hewlett-Packard Emulator Pods. Damage to the emulator circuitry may result if these precautions are not observed.

POWER DOWN TARGET SYSTEM.

Turn off power to the user target system and the emulation development station before inserting the user plug to avoid circuit damage resulting from voltage transients or mis-insertion of the user plug.

VERIFY USER PLUG ORIENTATION.

Make certain that Pin 1 of the target system microprocessor socket and Pin 1 of the user plug are properly aligned before inserting the user plug in the socket. Failure to do so may result in damage to the emulator circuitry.

PROTECT AGAINST STATIC DISCHARGE.

The emulator pod contains devices which are susceptible to damage by static discharge. Therefore, operators should take precautionary measures before handling the user plug to avoid emulator damage.

CAUTION

Chapter 3
PERFORMANCE VERIFICATION AND TROUBLESHOOTING

INTRODUCTION

Chapter three is arranged in two parts, Performance Verification and Troubleshooting. The scope of the performance verification is to detect problems at the board level only. Part II is restricted to a System and Subsystem Overview, and a Troubleshooting Flow Chart. Board level troubleshooting is in support of Hewlett-Packard's Bluestripe Exchange Program.

For convenience, the PV screens used in the Performance Verification are grouped together at the end of this section.

PERFORMANCE VERIFICATION

In a networked 64000 system (hard disk based), and in a stand-alone 64000 configuration (mini disk based), the Performance Verification software for the 64223A Emulator Control Card and the 64224A 80186 Emulator Pod is a subset of the option_test P.V. The option_test P.V. tests all possible option modules that can be configured within the expansion slots of the 64000 development station.

The following procedures explain how to run Performance Verification on the 64223A/64224A Emulation Subsystem for both a networked and a stand-alone 64000 system.

Other option cards connected to the emulator, such as memory control and analysis, have their own option_test software which tests the major functions of those cards but not interaction with other modules. To run Performance Verification on those option cards, refer to the service manual for the model number in question.

To test the 80186 emulator in a networked 64000 system, or in a stand-alone 64000 system, proceed as follows:

NOTE

If the 64000 system is a stand-alone configuration (mini disk based), then the following software modules must be contained on the current local disk system:

FLOPPY_OP_SYS
OPTION_TEST
PV_EMUL_80186

Other software modules may be necessary to perform other system functions.

Model 64224S
80186 Emulator Subsystem

Chapter 3
Performance Verification

a. Verify that the emulator is correctly installed in the development station and that the user probe is disconnected from the target system. (Refer to Chapter 2 for installation instructions.)

b. With the operating system initialized and awaiting a command, use the softkey or manually type the lower case command:

[option_test]   (RETURN)

See figure 3-1.

c. The P.V. will now display a directory of the installed option boards and their card slot number (figure 3-2). Locate the 80186 Emulator and enter the card slot number. For example, in figure 3-2 the 80186 Emulator is in card slot 8. Therefore, enter:

8   (RETURN)

d. A menu will now be displayed listing the four major tests available to exercise the 80186 Emulator (figure 3-3). Depress the *[cycle]* softkey. This will cause the performance verification software to cycle through the emulator P.V. tests. If no failures are observed, the 80186 Emulator operates correctly, and the testing may be terminated as described in the next paragraph. If a failure is observed, refer to the following sections for information on test operation and troubleshooting procedures.

e. To terminate execution of the Performance Verification, press the *[end]* softkey. This returns the display to the option_test Performance Verification card cage listing. If *[end]* is pressed at this level, the option_test Performance Verification is completely exited and the system is returned to the awaiting command status.

f. If further information is needed on the error results of each test, or you wish to execute only an individual test repeatedly, then the softkeys must be used to bring up the appropriate test display and begin test execution. The softkeys have the following actions:

[cycle]

Causes the performance verification software to execute each test on the display in turn; the inverse video bar will highlight each test name as the test is executed.

[disp_test]

When this softkey is pressed, the subtest display for the test name highlighted by the inverse video bar is put on screen. This subtest display shows all of the subtests and error status information for the particular test name.

[end]

This softkey, when pressed at the performance verification overview level (six major tests displayed), causes the testing to terminate at the end of the current cycle and returns the display to the option_test card slot listing. When *[end]* is pressed at this level, the performance verification software is exited entirely and the system is returned to the awaiting command status.

[exit_test]

This softkey, when pressed in the subtest display level, ends test execution at the end of the current cycle and returns the performance verification software to the next higher test display level.

[next_test]

Causes the inverse video bar to move to and highlight the next test name on the test display.

[option_test]

Causes the operating system to load the performance verification software and begin execution; the option_test card slot listing is displayed.

[print]

Causes all the information above the status line on the current test display to be copied to the system printer, if one is connected. The copy will not be done until the end of the current test cycle, if testing is in progress.

[<SLOT #>]

Pressing this softkey while in the option_test card slot listing display causes the system to prompt you for the slot number of the option module you wish to test.

[start]

Begins repeated execution of the test highlighted by the inverse video bar.

```
I/O BUS CONFIGURATION

ADRS   DEVICE
  0    7910 DISC MEMORY                    LU=0
  1    2631 PRINTER
  5    64100
  6    THIS 64100




STATUS:  Awaiting command           userid _____ 10:04
option_test_


   _____  _____  _____  _____  _____  _____  _____  _____
```

Figure 3-1. Awaiting Command Status

```
              HP 64000 Option Performance Verification
Slot #  ID #  Module
------  ----  ------
  7     0201H  Wide Memory Ctl.
  8     0032H  p80186 Emulator
  9     0102H  Wide Emul. Analysis




STATUS:  Awaiting option_test command _____13:03
8_

   ___end___  <SLOT #>  _____  _____  _____  _____  _____  _print_
```

Figure 3-2. Option_Test Card Slot Listing

```
                        80186 Performance Verification
    p80186 Emulator     in slot# 8          Wide Emul. Analysis in slot# 9
    Wide Memory Ctl.    in slot# 7

               Test                                    #Fails  #Tests

    Pod Register Tests (Static)                           0       0

    Pod Functionality Tests                               0       0

    Pod Register Tests (Dynamic)                          0       0

    Analysis Tests                                        0       0




    STATUS:  Awaiting option_test command _____13:17

    _

     __end__  __cycle__  next test disp test ____ ____ _____  print
```

Figure 3-3. 80186 Performance Verification

```
                        80186 Performance Verification
                          Pod Register Tests (Static)

               Test              Results  (Cumulative)  #Fails  #Tests
    PV Latches                    0000H       0000H        0       0

    Zero Comparator               0000H       0000H        0       0

    Monitor I/O Comparator        0000H       0000H        0       0

    Jam Ram                       0000H       0000H        0       0

    Mapper Ram                     000H        000H        0       0


    STATUS:  Awaiting option_test command _____13:21

    _

    _____  cycle  next test  start  exit test ____ _____  print
```

Figure 3-4. Pod Register Tests (Static)

```
                    80186 Performance Verification
                       Pod Functionality Test

         Test                   Address   Status   Data      #Fails  #Tests
1 - Reset Address               00000H    00H                  0       0
2 - Low Address                 00000H    00H                  0       0
3 - Run Status/Hold Proc.       00000H    00H                  0       0
4 - Halt Status                           00H                  0       0
5 - Address                     00000H    00H                  0       0
6 - Byte Operations                       00H      0000H       0       0
7 - Data Bits                             00H      0000H       0       0
8 - NMI (Low BPC break)         00000H    00H                  0       0



STATUS:  Awaiting option_test command _____13:23

    _

    _____  cycle   next test   start   exit test  _____  _____  print
```

Figure 3-5. Pod Functionality Test

```
                    80186 Performance Verification
                       Pod Register Tests  (Dynamic)

         Test                                            #Fails  #Tests

Jam Ram                                                    0       0

Monitor I/O Comparator                                     0       0




STATUS:  Awaiting option_test command _____13:24

    _

    _____  cycle   next test  disp test  exit test  _____  _____  print
```

Figure 3-6. Pod Register Tests (Dynamic)

Figure 3-7. JAM RAM Tests (Dynamic)

Figure 3-8. Pod Monitor I/O Tests (Dynamic)

```
                    80186 Performance Verification
        p80186 Emulator     in slot# 8          Wide Emul. Analysis in slot# 9
         Wide Memory Ctl.   in slot# 7

           Analysis Stimulus Test          Results  (Cumulative)     # Fail   # Test

        Analysis Trace                                                  0        0

        Address                        Address = 000000(000000)        0

        Data                               Data = 0000(0000)           0

        Status                       Status = 00000000(00000000)       0

        Analysis Break                                                 0

        STATUS:  Awaiting option_test command _____13:28

        _

        _____ _____ _____  start   exit test _____ _____  print
```

Figure 3-9. Analysis Stimulus Test

TARGET SYSTEM

EMULATION
POD

EMULATION BUS

POD BUS

EMULATION MEMORY BUS

AIMB

EMULATION
MEMORY
BOARD(S)

EMULATION
MEMORY
CONTROLLER

ADDITIONAL
ANALYSIS
MODULE

INTERNAL
ANALYSIS
MODULE

EMULATION
CONTROL
BOARD

BPC (MAINFRAME) BUS
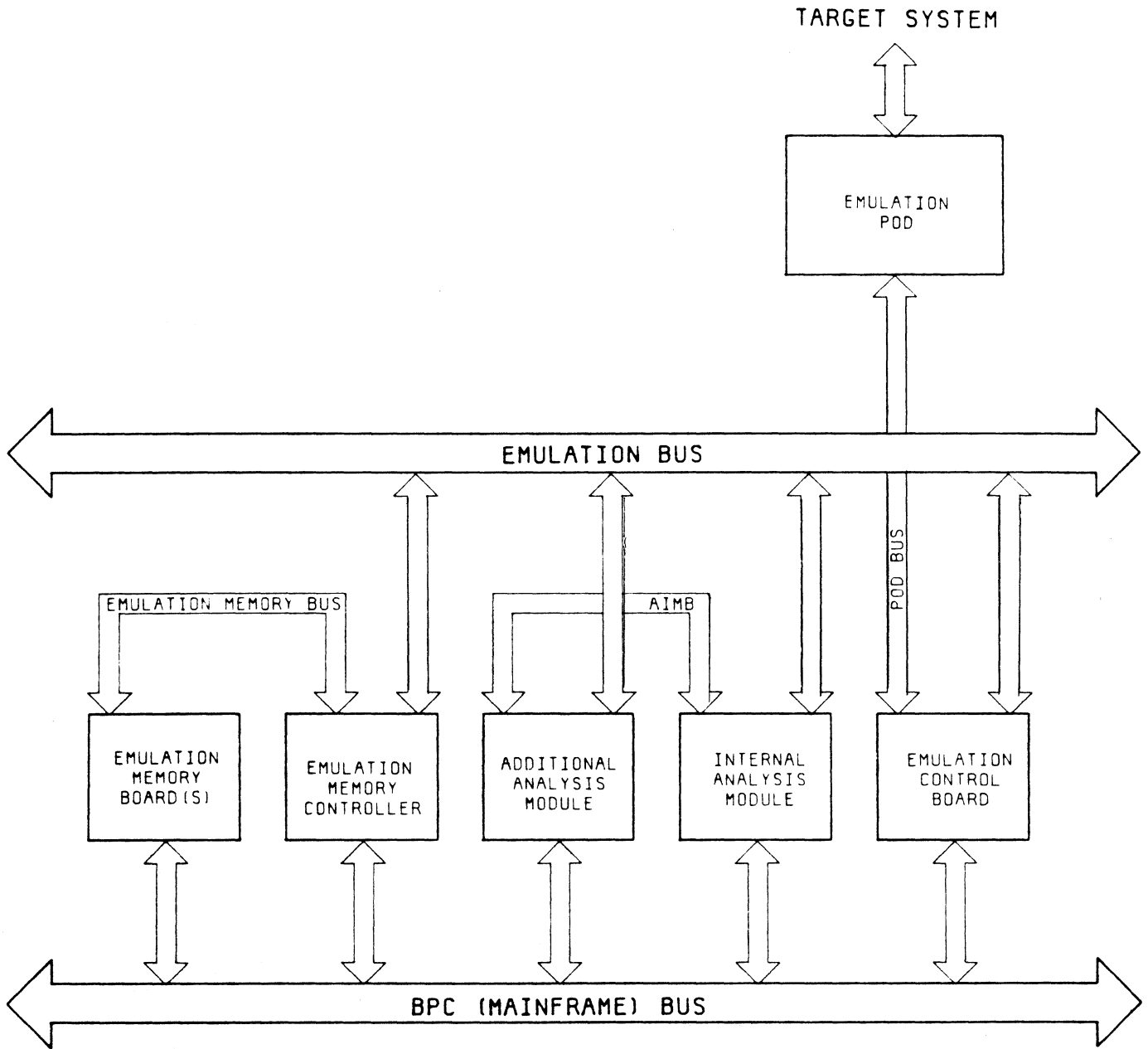
8/19/81

Figure 3-10. Emulation Subsystem

TROUBLESHOOTING

WHAT IS AN EMULATION SYSTEM?

Scope

Theory of operation for the 80186 emulator subsystem is restricted to an overview of emulation; a description of the emulation subsystem; and a description of the functional blocks of the emulator circuitry.

Emulation Overview

"Emulate" means to equal.   In the HP64000 Logic Development system, the emulation implementation allows the user to replace the microprocessor in the target system breadboard with a plug from the emulator pod. The plug appears to act as much like the emulated microprocessor as is possible within design constraints.

The user may develop programs using the assembler and compiler utilities of the 64000 system; store these on disk for later use; edit them as desired; and link them together while assigning absolute addresses (using the relocatable linker utility of the system). These programs may then be loaded into memory provided by the target system or by optional high-speed emulation memory boards resident within the development station.

Once the programs are loaded into memory, the user may then release the emulator to run them so that an evaluation of the software or firmware can be made. When problems are found, the causes may be diagnosed by requesting the emulator to single-step through the program, display its register, display a user or emulation memory location or locations, or perform other non-real time analysis functions. With the optional analysis module, real-time tracing of program state flow can be accomplished, providing a powerful tool for program analysis and debugging.

The emulation processor actually accomplishes the non-real time functions listed above. This is done by linking an emulation monitor program into the user's code loaded into memory. The emulation processor may alternately execute from the actual user's program or from the emulation monitor routines as necessary to perform the emulation functions.

For example, if the user wishes to display the contents of the processor's registers, the mainframe CPU asserts a break request to the emulator. The emulator control card will then respond by jamming a series of instructions onto the processor's bus which cause the processor to jump into monitor code execution. After dumping register contents into emulation memory, the processor is then returned to the location in the user's program immediately following the location it was executing when the break request occurred. The mainframe CPU can now access the contents of emulation memory to read the register contents and display them on screen.

Emulation Subsystem Overview

GENERAL. Figure 3-10 shows a block diagram of the emulation subsystem. The subsystem provides emulation of a selected microprocessor in the user's target system. Capabilities include software development and debugging, hardware simulation, and real-time program execution.

EMULATOR POD. The Emulator Pod contains the specific microprocessor to be emulated. It may be used without a target system for software development; or its user plug may replace the microprocessor in the target system, allowing execution of software developed on the 64000 system. The pod communicates with the rest of the emulation subsystem via the pod bus.

EMULATION CONTROL CARD. The Emulation Control Card performs the interface functions between the emulator pod, the emulation bus, and the mainframe bus. It buffers and controls data transactions between these three buses; performs a memory mapping function which is used to control buffers within the emulator pod and control board, and records various pieces of status information. It also contains the background memory, which is used by the mainframe CPU to control the emulation subsystem.

INTERNAL ANALYSIS. The Internal Analysis module continuously stores data present on the emulation bus. It may be requested to store only certain sequences or types of data, and start or stop a store based upon the type of information present on the bus. The trace storage buffer is able to contain 256 different program states. A software disassembly function is also provided which converts binary information stored on the analysis board to instruction mnemonics, then displays them on the 64000 CRT at the user's request.

EMULATION MEMORY CONTROLLER. The Emulation Memory Controller is used to control access to emulation memory and perform a mapping function, which allows various blocks of memory to appear to reside at user selected address ranges and respond as different types of memory (ROM, RAM, undefined).

EMULATION MEMORY. The Emulation Memory board(s) consist of banks of RAM in multiples of 32K. Access to this memory is controlled by the emulation memory controller.

Emulator Block Diagrams

EMULATOR CONTROL CARD. Figure 3-11 is a block diagram of the emulator control card.

The emulator control card is essentially an interface mechanism. It controls communication between the mainframe CPU (host processor), the emulator pod, the memory control bus, and the analysis bus.

Address information from the emulator pod is latched by the Pod Address Latch on each occurrence of the ALE (Address Latch Enable) strobe from the emulator pod. The latched address information is transmitted directly to the emulation memory controller bus for use in addressing emulation memory locations after translation by the memory controller mapper RAM. In addition, the address information stored in the Pod Address Latch may be transmitted directly to the analysis address bus through the Analysis Address Buffers if the user has selected analysis of processor operation by bus cycle rather than by executed opcode bytes. The Last Address Latch may capture selected addresses if necessary for further interpretation by the user. This is done on receipt of a break request so that the cause of the break can be determined.

Data communications between the pod and the emulation interfaces is carried out through the Memory Bus Data Transceivers. These transceivers are controlled by signals from the emulator

pod and the emulator control board. Typically, the emulation processor determines the orientation of these transceivers as it carries out read and write transactions with emulation memory. However, in some instances the mainframe CPU must write data to the emulator pod registers to set up default execution conditions or read data from the pod registers during performance verification.

To accomplish communications with the pod registers, two additional sets of buffers come into play. These are the Mainframe Data Transceivers and the Mainframe to Memory Bus Data Transceivers. The Mainframe Data Transceivers are controlled by logic driven by the mainframe CPU and buffer all data transactions between emulator circuitry and the mainframe CPU. The Mainframe to Memory Bus Data Transceivers are controlled jointly by the emulator control card and the emulator pod; they buffer the reads and writes of the emulator pod registers initiated by the mainframe.

In addition to communications with the emulator pod data bus, the Mainframe Data Transceivers buffer writes and reads of other emulator control card circuits. The ID Buffer provides an identification of the emulator to the mainframe upon request. The Emulator Status Buffer drives miscellaneous status information from the emulator pod and the control board to the mainframe CPU. This information allows the emulation software to determine whether or not the processor is executing bus cycles; whether it is in a bus grant, wait, or halted state, and whether or not the emulator pod is inserted into a powered up target system. The Emulator Control Register allows programming of various emulator pod options by the mainframe CPU. These options allow the user to reset the processor or request a hardware break and determine the mode of emulation analysis traces (all bus cycles or executed opcodes only). The Mainframe Control Logic orchestrates all these operations by providing the proper function selection and timing signals to complete the transaction.

Data from the emulator pod is also provided to the inputs of the analysis data buffers. The buffers drive information from the pod data bus to the analysis data bus continuously if the bus cycle mode of analysis tracing has been selected; otherwise, the buffers are tri-stated.

Three separate strobe generators translate timing signals provided by the emulator pod to the signals required by the emulation memory controller and emulation analysis buses. The Memory Strobe Generator observes status and timing information from the pod to determine when the emulation processor will be using emulation memory; when memory is in use, the circuit must send out the proper write strobe (if necessary) and determine which bytes (upper, lower, or both) of memory should be enabled. The analysis strobe generator uses status information from the pod along with the byte strobes and some internal signals from the memory strobe generator to determine when the analysis clock and analysis byte strobes should be activated. The queue tracking circuitry strobe generator uses the queue status information from the emulation processor and a timing clock from the pod to generate certain timing signals which control the emulator control board's queue image circuitry.

The queue image circuitry replicates the emulation processor's internal instruction queue so that proper analysis tracking of emulator instruction execution can be done. Note the implications of this: if analysis tracing of all bus cycles is selected by the user, then all bus cycles initiated by the emulation processor are sent to the analysis bus through the analysis address and data bus buffers described previously; if analysis tracing of only executed opcodes is to be done, then the queue image circuitry takes over and determines when the analysis module should be clocked and what information should be provided to it.

Instruction Fetch Latches monitor the memory data bus continuously. If the current cycle is an instruction fetch, these latches are clocked and the opcode is stored. The queue image RAM (an FIFO buffer) accepts this opcode at the bottom of it's stack and pushes any other opcodes

currently present up towards the top of the stack. The queue tracking strobe generator clocks each byte from this stack out to the executed byte latches as the emulation processor actually executes that byte. The Executed Byte Latches drive the analysis data bus.

In addition to the queue replication circuitry, the program counter of the processor must be replicated in hardware. This is done by the 18X Program Counter Image, which consists of a 20 bit counter circuit clocked by the Queue Tracking Circuitry Strobe Generator. The counter is clocked once each time an instruction fetch occurs; the output of the counters is enabled onto the analysis address bus when the fetched opcode is actually executed.

Analysis status information is provided by the Analysis Status Buffer and the Analysis Status Multiplexer. The Analysis Status Buffer drives the multiplexed upper address/status bits to the analysis status bus at all times if bus cycle analysis mode is selected; otherwise, it is off. The Analysis Status Multiplexer provides the standard status information from the emulation processor to the analysis status bus if bus cycle analysis mode is selected; otherwise, it provides information about queue usage by the emulation processor (indicates first byte fetched from queue).
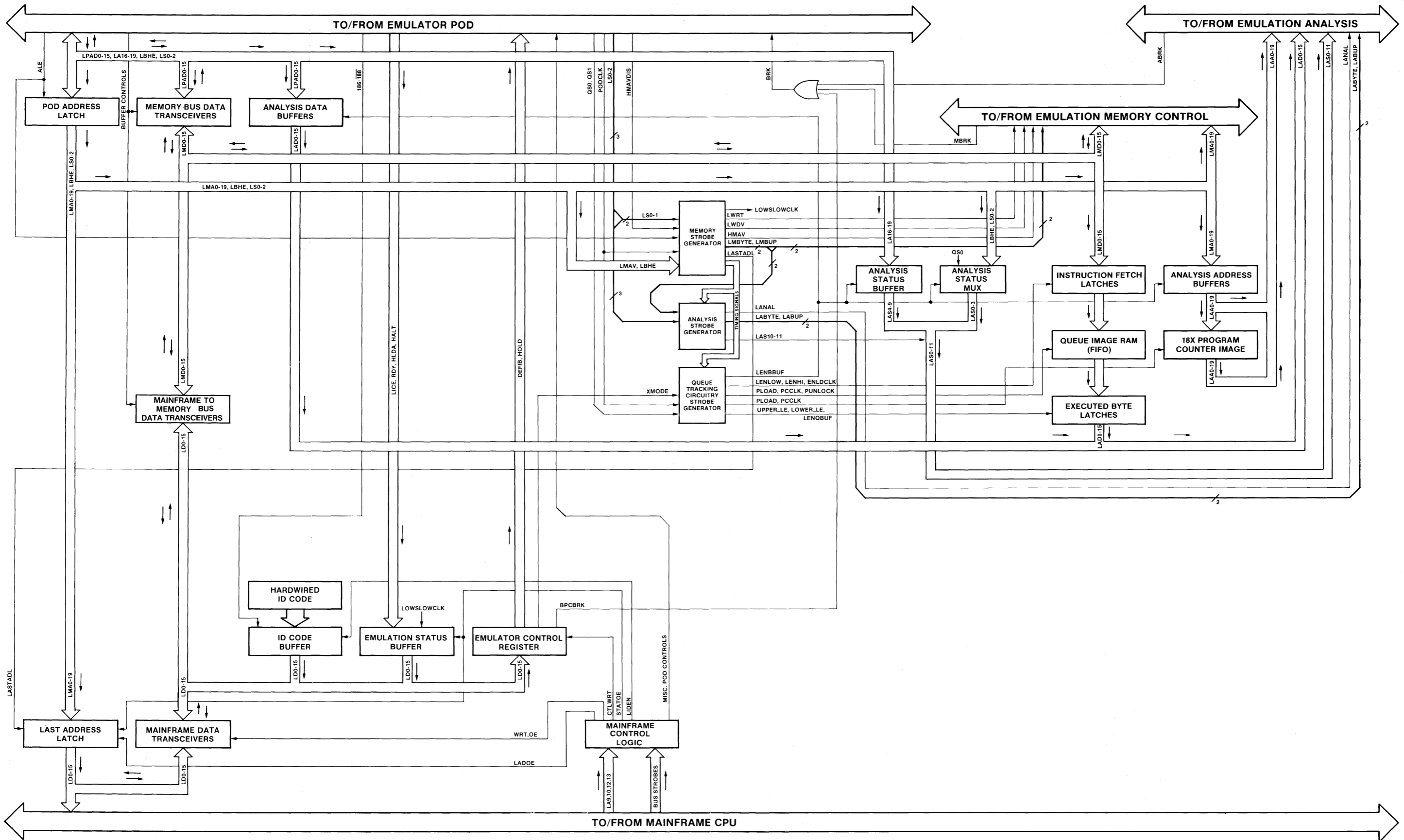
Figure 3-11.
8018X Emulator Control Card Block Diagram

EMULATOR POD. Figure 3-12 is a block diagram of the emulator pod. The emulator pod contains the 80186 microprocessor and circuits necessary to control the operation of that processor.

The interface between the 80186 microprocessor and the user target system is fully buffered to reduce the possibility of loading the user's system. Transceivers drive address, data and status information to and from the user system. Note that the upper address and status information can be driven both to and from the user system. This allows DMA operations to emulation memory contained inside the development station from the user system.

All the chip select and timer output signals produced by the microprocessor are buffered and sent directly to the target system.

The DMA request, timer inputs, and interrrupt request signals from the target system are buffered and sent to the processor only if the emulator pod is in circuit. This prevents noise on these lines from erroneously triggering the processor's functions when the pod is out of circuit.

Sensing of the in-circuit condition is accomplished by the HICE detector. This consists of a low pass filter and a logic buffer which are driven by the user's +5 volt power input to the processor socket. Approximately 20 mA of current (see electrical characteristics in Chapter One) is pulled from the user's system to accomplish this sense function.

The timing reference for the emulation microprocessor is provided by the Clock Selection/Clock Generation Circuit. An internal oscillator of 16 MHz frequency is provided along with a crystal driver and a logic selection circuit. The crystal driver is used if the user provides an external crystal in his target system; in this case, the driver provides sufficient power to cause the crystal to oscillate. The selection circuit is used during the emulation configuration steps to determine whether the internal oscillator or the external clock source will be sent to the microprocessor.

Description of the 80186 microprocessor is beyond the scope of this manual. Please refer to the microprocessor manufacturer's documentation for further information concerning the processor.

The 80186 processor may be selected to either provide cycle strobe information or queue status information, depending on what is done with the READ line. If the READ line is grounded, the processor provides queue status information, and the S0-2 lines must be decoded to provide the correct READ, WRITE, and cycle start information. Otherwise, the processor puts out ALE, READ, and WRITE as necessary to perform memory and I/O bus transactions.

The processor within the emulator pod is constantly run in the queue status mode. This allows external replication of the instruction queue (accomplished on the emulation control card) which provides additional information for analysis. The S0-2 lines are decoded to provide the proper READ, WRITE and ALE timing strobes to the user system. However, should the user decide to run his system in the queue status mode, some changes must be made. This function is accomplished by the Processor Mode Detector. The Mode Detector senses the state of the user's READ line while in circuit and determines what to send the user system: either the queue status lines QS0 and QS1; or the READ, WRITE and ALE strobes.
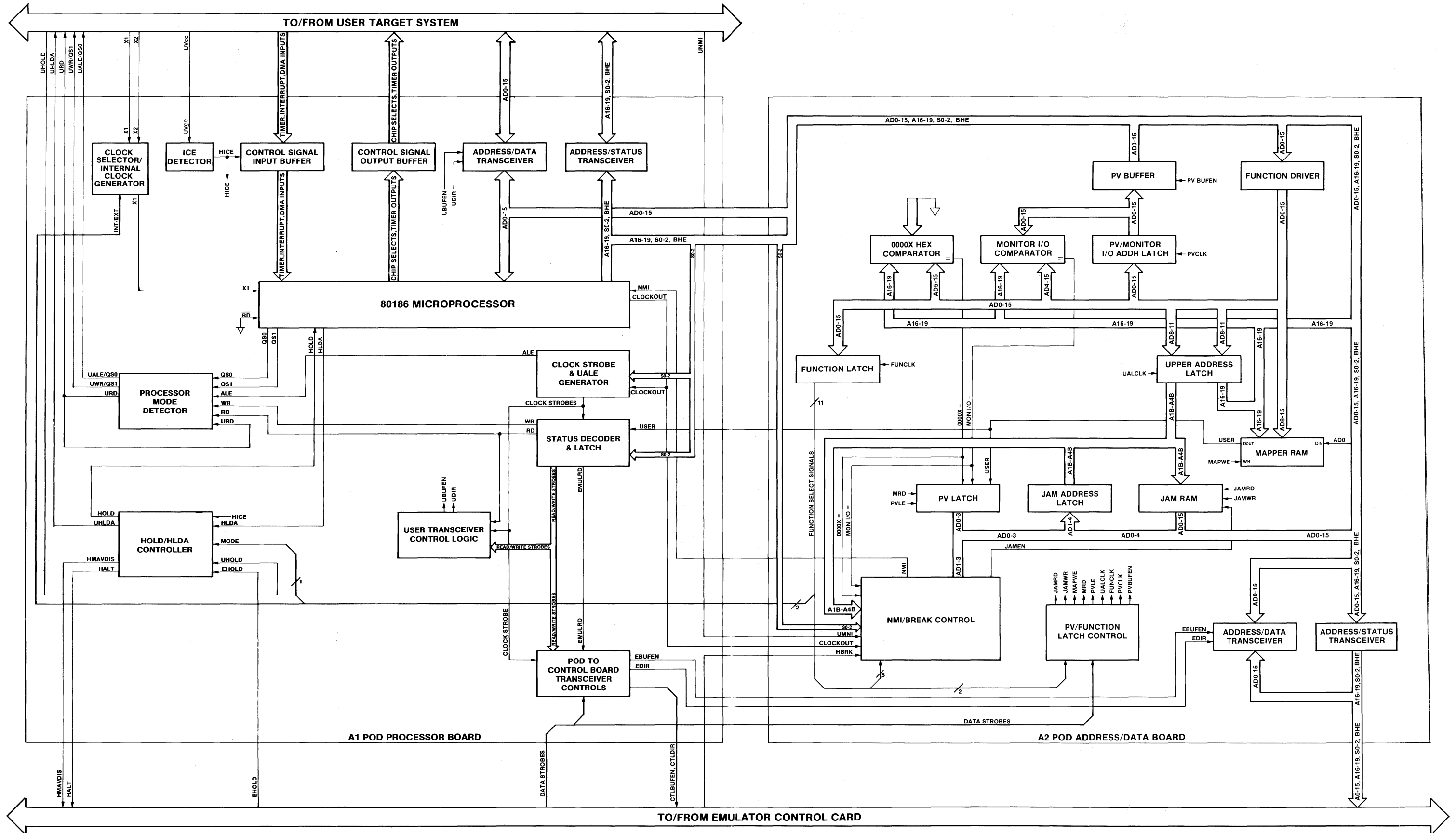
Figure 3-12.
80186 Emulator Pod Block Diagram
3-16

The Hold/Hlda controller arbitrates between user bus grant requests and emulation bus grant requests. The user may need the bus to perform some DMA transaction, such as loading display memory. The emulation bus request is generated when the mainframe CPU within the development station needs to access emulation memory without interference from emulation processor bus cycles. (This would occur, for example, when the user wanted a dynamic display of emulation memory locations on the development station CRT.) The Hold/Hlda controller determines who should receive the bus, requests the processor to release it, and then informs the proper system (user or emulation) whether or not the request was successful.

The Clock Strobe and UALE generator uses the clock output from the emulation processor and the status outputs to generate timing strobes used in the transceiver controls and the status decoder. In addition, the address latch enable signal is recreated by this circuitry to decode the multiplexed address/data bus.

The Status Decoder/Latch circuitry decodes the status information from the emulation processor into read and write strobes which are latched for use by the transceiver controls. The read and write strobes are further qualified by the USER signal from the A2 board Mapper RAM to determine whether the current cycle accesses the user system or the emulation system.

The User Transceiver Control Logic uses the read and write strobes from the Status Decoder and the clock strobes to control the tri-state address/data transceivers at the user system interface. Both output enable and direction controls are driven from this circuit.

The Pod to Control Board Transceiver Controls circuit also uses the read/write signals from the Status Decoder and various clock strobes; in addition, read/write strobes from the emulation control board are input to this circuitry. The outputs control the tri-state transceivers on the pod A2 board which communicate address and data information between the pod and control board.

Orientation of the transceivers is usually driven by requirements of the emulation processor's bus cycles. However, during emulation configuration and pod performance verification, the read/write strobes from the emulation control card are the primary determinant of transceiver orientation.

The Function Drivers are buffers which constantly drive the pod address/data information into various circuits on the pod A2 board. Of primary importance during performance verification are the PV/Monitor I-O latches. These latches are clocked during every PV write cycle; the latch outputs can be read back by the control board through the PV buffers and the Address/Data Transceivers.

A secondary function of these latches is programming of the Monitor I/O comparator address. This is done during emulation configuration. An address value is programmed into the latches; when the monitor is entered or exited during emulation runs, the equality output of the comparator will be asserted. The information is used by the NMI/Break Control Circuitry.

The 0000X Hex Comparator detects bus cycles which enter the processor pointer section of memory; one set of inputs into this comparator is grounded; the other set of inputs is driven by address bits 5 through 19. The equality output bit is used by the NMI/Break Control Circuit.

The Function Latch is used to program various processor configurations. Examples include: internal or external clock to drive processor; selection of which performance verification latch to read; priority of user non-maskable interrupts over emulation breaks; and so on. The latch is programmed with address/data bits 0-15 from the Function Driver.

The Upper Address Latch is used during emulation configuration and performance verification. The latch is loaded with the values of AD8-11 and used to drive the address inputs of the Jam RAM and the upper address inputs of the Mapper RAM.

The Mapper RAM is used for transceiver control. The RAM is programmed during emulation configuration to indicate which area various memory address ranges will be assigned to; the area assigned can only be the user system or the emulation system. During emulation runs, the data output (USER signal) will indicate where each address resides as that address is put on the bus.

The Jam RAM is programmed during emulation configuration with instructions to be used during an emulation break sequence. When a break occurs, the NMI/Break Controller will drive the RAM's address bus in such a way as to force the instructions onto the bus. These instructions will cause the processor to enter the emulation monitor and begin execution there.

The Jam Address Latch contains the address value of the next RAM instruction during a break sequence.

The PV latch is used during performance verification to make sure that the Mapper RAM USER output is responding correctly; and that the two comparator equality outputs are responding as expected.

The PV/Function Latch Control is driven by two register select bits from the Function Latch along with data strobes from the emulation control card. The outputs determine which ports or RAM address on the pod A2 board should be programmed or read during the current bus cycle.
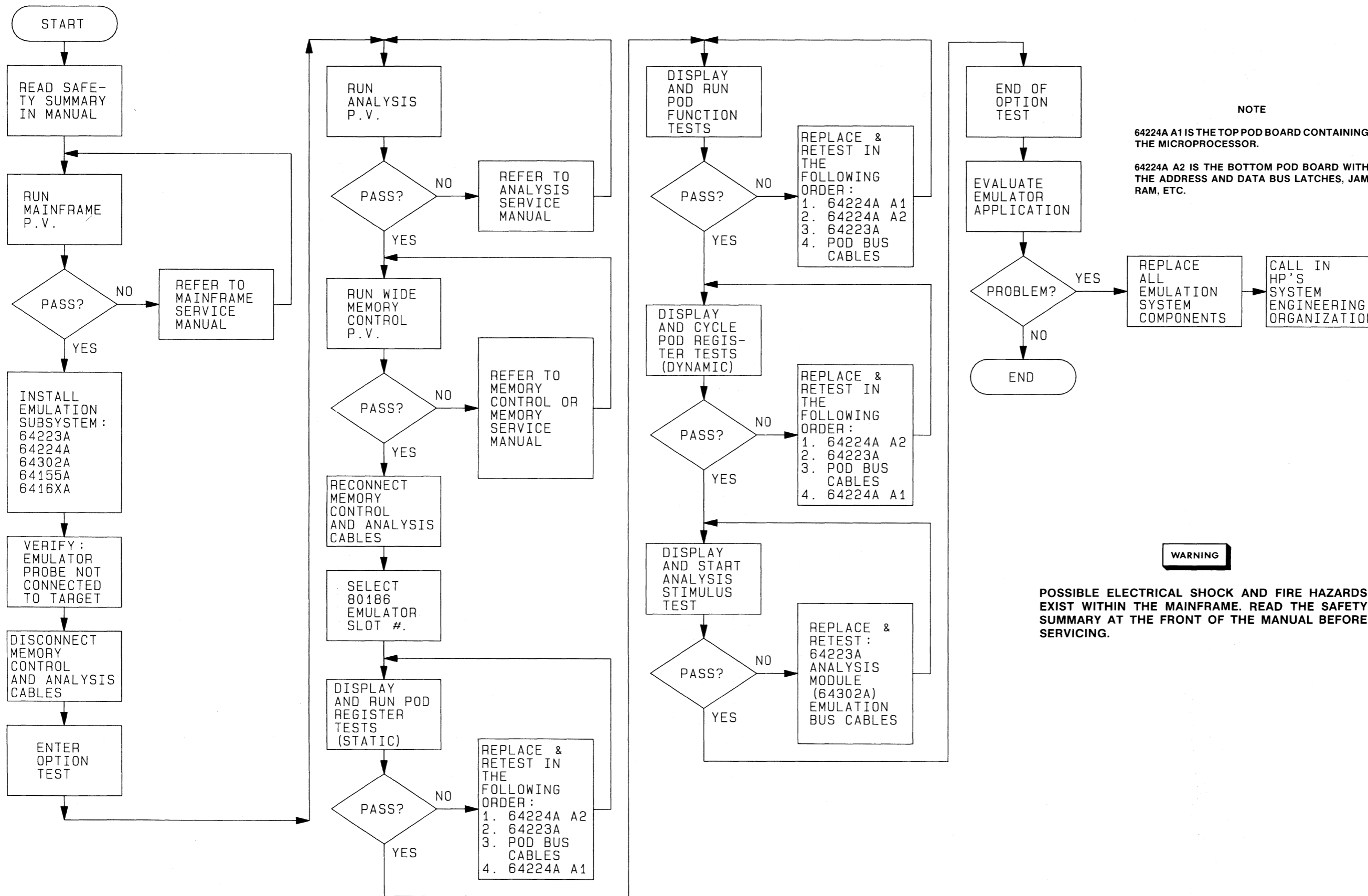
The NMI/Break Control circuit uses the NMI input from the user system and the BRK request line from the emulation control card to drive the NMI input to the processor in a controlled fashion. The LUNMIPR input line from the function latch determines which request has priority. If a user NMI request occurs, it will be processed in a normal fashion. If an emulation break request occurs, the NMI to the processor is asserted and instructions are jammed onto the bus which cause the processor to enter the emulation monitor.

TROUBLESHOOTING FLOW CHART

Figure 3-13 is a troubleshooting flowchart for the 80186 emulator subsystem. When using the flowchart:

a. If you need more specific instructions on running performance verification or interpreting the test results, refer to part one in this chpater.

b. A block marked "Replace & Retest" on the flowchart, followed by a list of assemblies, indicates that each assembly should be replaced one at a time in that order and the emulation subsystem should be retested after each replacement.

c. Servicing of the emulator circuitry should only be performed by qualified personnel aware of the hazards involved. Read the safety summary at the front of this manual for further details on safety precautions to be taken while servicing this instrument.

START

READ SAFE-
TY SUMMARY
IN MANUAL

RUN
MAINFRAME
P.V.

PASS? — NO → REFER TO
MAINFRAME
SERVICE
MANUAL

YES

INSTALL
EMULATION
SUBSYSTEM:
64223A
64224A
64302A
64155A
6416XA

VERIFY:
EMULATOR
PROBE NOT
CONNECTED
TO TARGET

DISCONNECT
MEMORY
CONTROL
AND ANALYSIS
CABLES

ENTER
OPTION
TEST

RUN
ANALYSIS
P.V.

PASS? — NO → REFER TO
ANALYSIS
SERVICE
MANUAL

YES

RUN WIDE
MEMORY
CONTROL
P.V.

PASS? — NO → REFER TO
MEMORY
CONTROL OR
MEMORY
SERVICE
MANUAL

YES

RECONNECT
MEMORY
CONTROL
AND ANALYSIS
CABLES

SELECT
80186
EMULATOR
SLOT #.

DISPLAY
AND RUN POD
REGISTER
TESTS
(STATIC)

PASS? — NO → REPLACE &
RETEST IN
THE
FOLLOWING
ORDER:
1. 64224A A2
2. 64223A
3. POD BUS
   CABLES
4. 64224A A1

YES

DISPLAY
AND RUN
POD
FUNCTION
TESTS

PASS? — NO → REPLACE &
RETEST IN
THE
FOLLOWING
ORDER:
1. 64224A A1
2. 64224A A2
3. 64223A
4. POD BUS
   CABLES

YES

DISPLAY
AND CYCLE
POD REGIS-
TER TESTS
(DYNAMIC)

PASS? — NO → REPLACE &
RETEST IN
THE
FOLLOWING
ORDER:
1. 64224A A2
2. 64223A
3. POD BUS
   CABLES
4. 64224A A1

YES

DISPLAY
AND START
ANALYSIS
STIMULUS
TEST

PASS? — NO → REPLACE &
RETEST:
64223A
ANALYSIS
MODULE
(64302A)
EMULATION
BUS CABLES

YES

END OF
OPTION
TEST

EVALUATE
EMULATOR
APPLICATION

PROBLEM? — YES → REPLACE
ALL
EMULATION
SYSTEM
COMPONENTS → CALL IN
HP'S
SYSTEM
ENGINEERING
ORGANIZATION

NO

END

NOTE

64224A A1 IS THE TOP POD BOARD CONTAINING
THE MICROPROCESSOR.

64224A A2 IS THE BOTTOM POD BOARD WITH
THE ADDRESS AND DATA BUS LATCHES, JAM
RAM, ETC.

WARNING

POSSIBLE ELECTRICAL SHOCK AND FIRE HAZARDS
EXIST WITHIN THE MAINFRAME. READ THE SAFETY
SUMMARY AT THE FRONT OF THE MANUAL BEFORE
SERVICING.

Figure 3-13.
80186 Emulator Troubleshooting Flowchart
3-20

Chapter 4
ADJUSTMENTS

The Model 64224S 80186 Emulator Control Card has no adjustments.

NOTES

Chapter 5
REPLACEABLE PARTS

INTRODUCTION

This chapter contains information for ordering parts. Table 5-1 lists abbreviations used in the parts list and throughout the manual. Table 5-2 lists all replaceable parts in reference designator order.

EXCHANGE ASSEMBLIES

The components of the Model 64224S are supported through the Hewlett-Packard Corporate Parts Center on the Bluestripe Exchange Program. Exchange, factory repaired and tested assemblies are available only on a trade-in basis; therefore, assemblies required for spare parts stock must be ordered using the new assembly part number. Part numbers for both new and exchange assemblies may be found in table 5-2, Replaceable Parts.

ABBREVIATIONS

Table 5-1 lists abbreviations used in the parts list, schematics, and throughout the manual. In some cases, two forms of the abbreviation are used: one all in capital letters, and one partial or no capitals. This occurs because the abbreviations in the parts list are always capitals. However, in the schematics and other parts of the manual, other abbreviation forms are used with both lowercase and uppercase letters.

REPLACEABLE PARTS LIST

Table 5-2 is the list of replaceable parts and is organized as follows:

    a. Chassis-mounted parts in alphanumerical order by reference designation.

    b. Electrical assemblies and their components in alphanumerical order by reference designation.

    c. Miscellaneous.

The information given for each part consists of the following:

    a. The Hewlett-Packard part number and the check digit.

    b. The total quantity (Qty) in the instrument.

    c. The description of the part.

The total quantity for each part is given only once - at the first appearance of the part number in the list.

ORDERING INFORMATION

To order a part listed in the replaceable parts table, quote the Hewlett-Packard part number and check digit, indicate the quantity required, and address the order to the nearest Hewlett-Packard office.

To order a part that is not listed in the replaceable parts table, include the instrument model number, instrument repair number, the description and function of the part, and the number of parts required. Address the order to the nearest Hewlett-Packard office.

DIRECT MAIL ORDER SYSTEM

Within the USA, Hewlett-Packard can supply parts through a direct mail order system. Advantages of using the system are as follows:

    a. Direct ordering and shipment from the HP Parts Center in Mountain View, California.

    b. No maximum or minimum on any mail order (there is a minimum order amount for parts ordered through a local HP office when the orders require billing and invoicing).

    c. Prepaid transportation (there is a small handling charge for each order).

    d. No invoices - to provide these advantages, a check or money order must accompany each order.

Mail-order forms and specific ordering information are available through your local HP office. Addresses and phone numbers are located at the back of this manual.

POD BUS
CABLES (NOT INCLUDED
WITH 64223A)

W1 (EMULATION MEMORY
CONTROLLER CABLES)

MP2
(EXTRACTOR - "64223A")

MP3
(EXTRACTOR - "EM8018X")

MP1
(PIN)

MP1 (PIN)

A1 (BOARD ASSEMBLY)
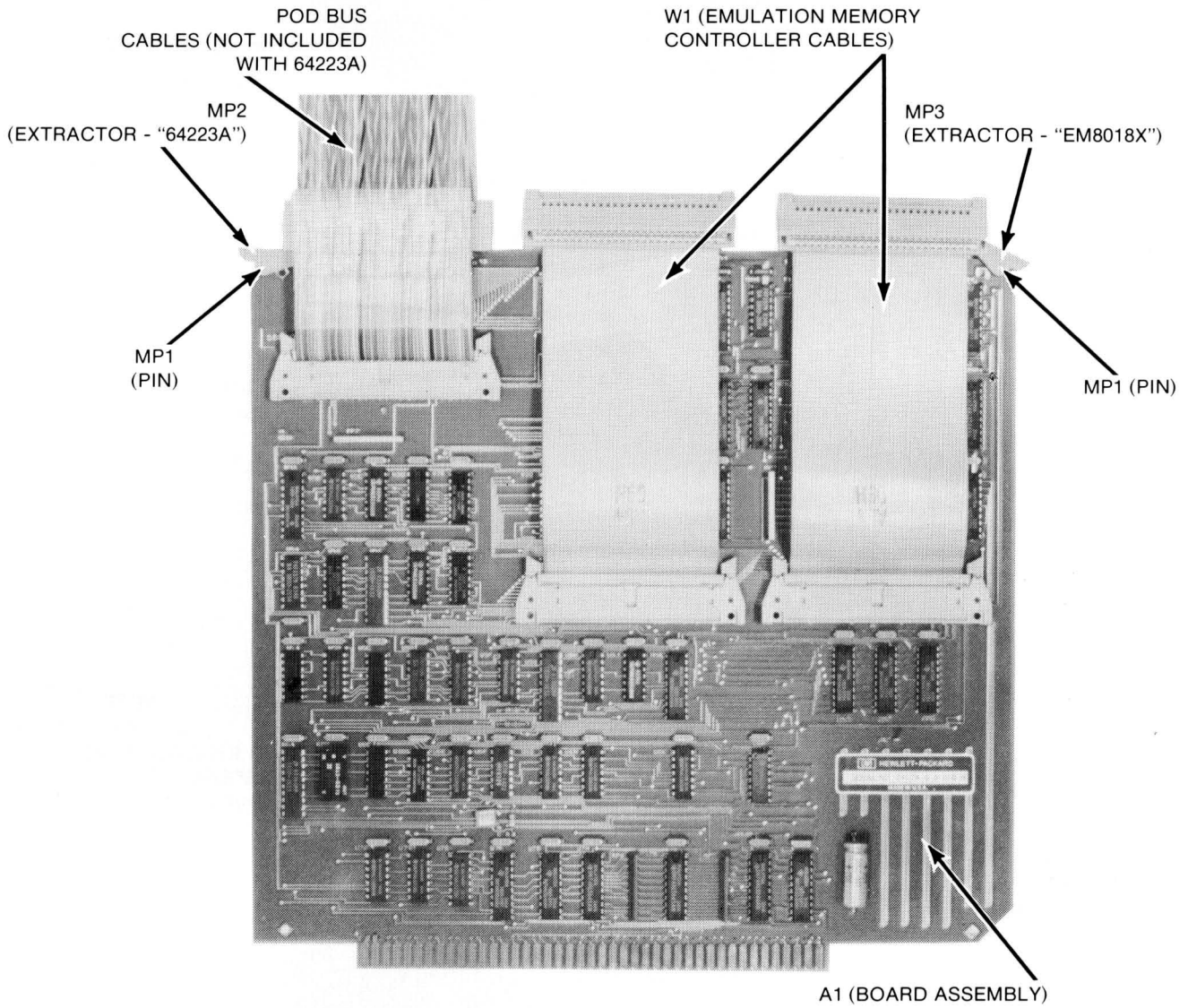
Figure 5-1. 64223A 8018X Emulator Control Card Parts Locator
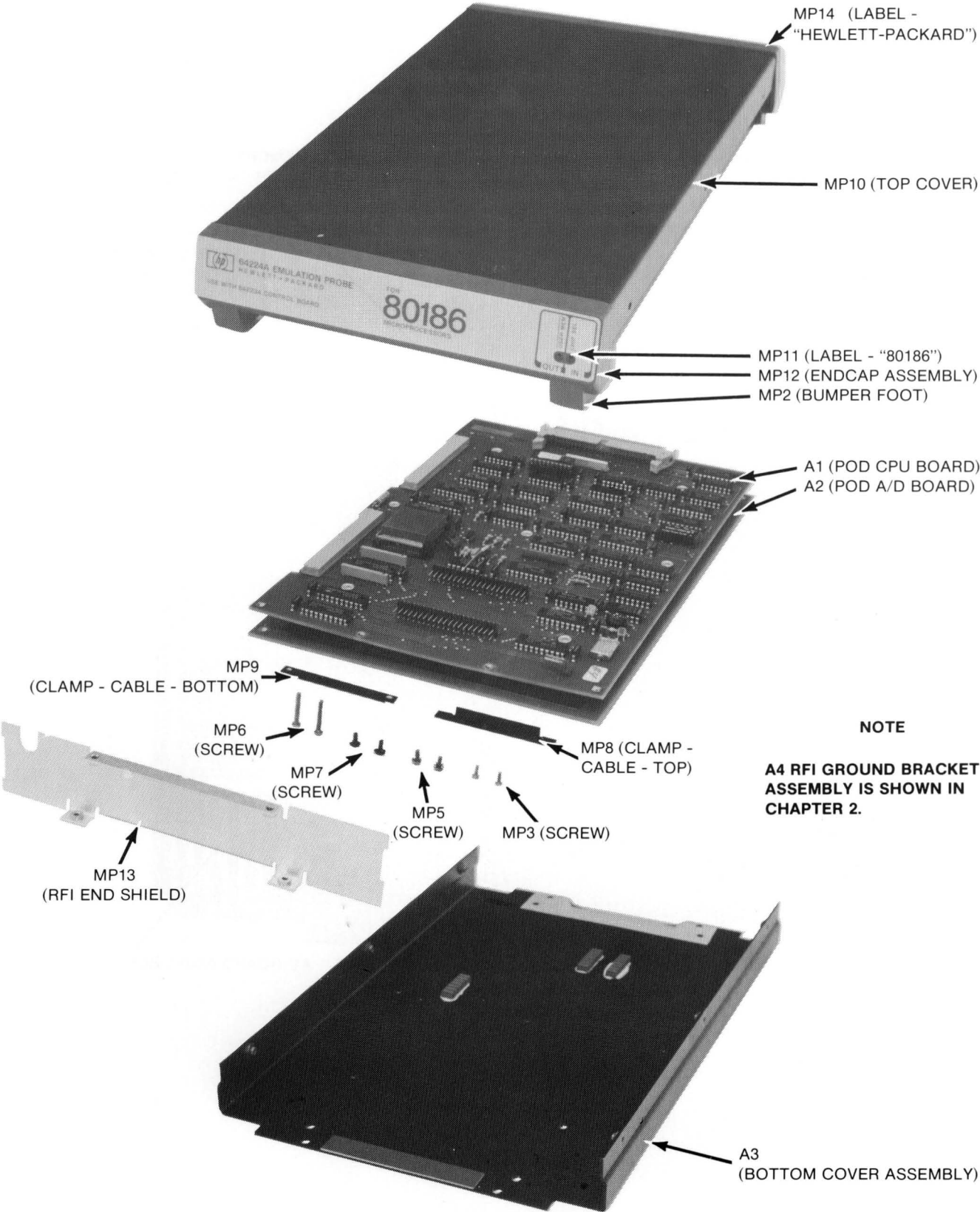
MP14 (LABEL - "HEWLETT-PACKARD")

MP10 (TOP COVER)

MP11 (LABEL - "80186")
MP12 (ENDCAP ASSEMBLY)
MP2 (BUMPER FOOT)

A1 (POD CPU BOARD)
A2 (POD A/D BOARD)

MP9
(CLAMP - CABLE - BOTTOM)

MP6
(SCREW)

MP8 (CLAMP - CABLE - TOP)

MP7
(SCREW)

MP5
(SCREW)

MP3 (SCREW)

MP13
(RFI END SHIELD)

NOTE

**A4 RFI GROUND BRACKET
ASSEMBLY IS SHOWN IN
CHAPTER 2.**
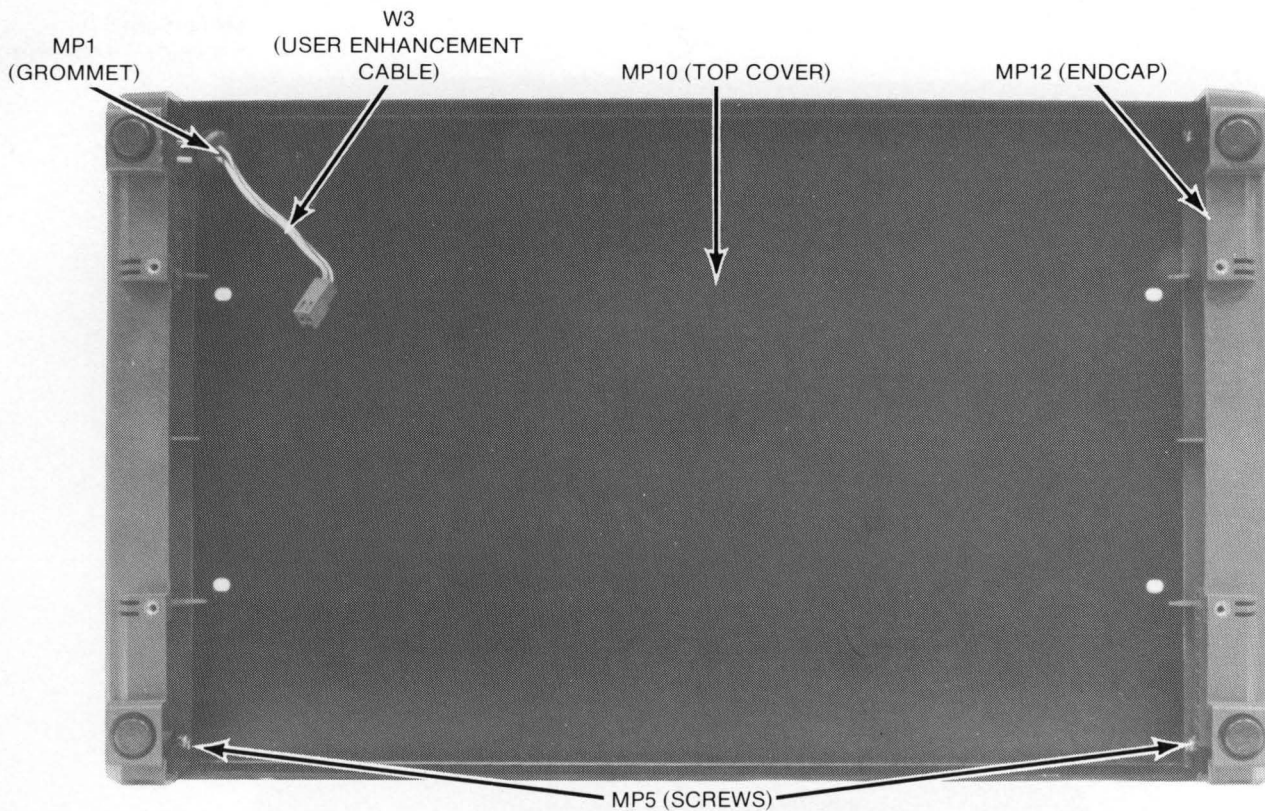
A3
(BOTTOM COVER ASSEMBLY)

Figure 5-2. 64224A 80186 Emulator Pod Illustrated Parts Breakdown (Sheet 1 of 4)

MP1
(GROMMET)

W3
(USER ENHANCEMENT
CABLE)

MP10 (TOP COVER)

MP12 (ENDCAP)

MP5 (SCREWS)

A3 BOTTOM COVER ASSEMBLY

A3MP2
(TRIM)

A3MP4
(HEAT CONDUCTIVE
ADHESIVE)

A3MP3
(HEAT SINK -
RUBBER)

A3MP1
(BOTTOM COVER -
SHEET METAL ONLY)

Figure 5-2. 64224A 80186 Emulator Pod Illustrated Parts Breakdown (Sheet 2 of 4)

MP14 (LABEL -
"HEWLETT-PACKARD")

MP11
(LABEL - "80186")

MP7 (SCREWS)

MP5 (SCREWS)

MP6 (SCREWS)

Figure 5-2. 64224A 80186 Emulator Pod Illustrated Parts Breakdown (Sheet 3 of 4)

W1 (USER CABLE)

W4, W5
(PROBE LEAD ASSEMBLIES)

MP4
(GRABBER
ASSEMBLIES)

A1 (POD CPU BOARD)

W2 (POD BUS CABLE)

W1
(USER CABLE)

MP8 (TOP CABLE
CLAMP) (MP9,
BOTTOM CABLE CLAMP,
NOT SHOWN)

MP3 (SCREW)

W1
(USER CABLE)

W2
(POD BUS CABLES)

A2 (POD
A/D BOARD)

Figure 5-2. 64224A 80186 Emulator Pod Illustrated Parts Breakdown (Sheet 4 of 4)

Table 5-1. Reference Designators and Abbreviations

REFERENCE DESIGNATORS

A	= assembly	F	= fuse	MP	= mechanical part	U	= integrated circuit
B	= motor	FL	= filter	P	= plug	V	= vacuum, tube, neon bulb, photocell, etc
BT	= battery	IC	= integrated circuit	Q	= transistor		
C	= capacitor	J	= jack	R	= resistor	VR	= voltage regulator
CP	= coupler	K	= relay	RT	= thermistor	W	= cable
CR	= diode	L	= inductor	S	= switch	X	= socket
DL	= delay line	LS	= loud speaker	T	= transformer	Y	= crystal
DS	= device signaling (lamp)	M	= meter	TB	= terminal board	Z	= tuned cavity network
E	= misc electronic part	MK	= microphone	TP	= test point		

ABBREVIATIONS

A	= amperes	H	= henries	N/O	= normally open	RMO	= rack mount only
AFC	= automatic frequency control	HDW	= hardware	NOM	= nominal	RMS	= root-mean square
AMPL	= amplifier	HEX	= hexagonal	NPO	= negative positive zero (zero temperature coefficient)	RWV	= reverse working voltage
		HG	= mercury				
BFO	= beat frequency oscillator	HR	= hour(s)				
BE CU	= beryllium copper	HZ	= hertz	NPN	= negative-positive-negative	S-B	= slow-blow
BH	= binder head					SCR	= screw
BP	= bandpass			NRFR	= not recommended for field replacement	SE	= selenium
BRS	= brass	IF	= intermediate freq			SECT	= section(s)
BWO	= backward wave oscillator	IMPG	= impregnated	NSR	= not separately replaceable	SEMICON	= semiconductor
		INCD	= incandescent			SI	= silicon
CCW	= counter-clockwise	INCL	= include(s)			SIL	= silver
CER	= ceramic	INS	= insulation(ed)	OBD	= order by description	SL	= slide
CMO	= cabinet mount only	INT	= internal	OH	= oval head	SPG	= spring
COEF	= coeficient			OX	= oxide	SPL	= special
COM	= common	K	= kilo=1000			SST	= stainless steel
COMP	= composition					SR	= split ring
COMPL	= complete	LH	= left hand	P	= peak	STL	= steel
CONN	= connector	LIN	= linear taper	PC	= printed circuit		
CP	= cadmium plate	LK WASH	= lock washer	PF	= picofarads= 10^{-12} farads	TA	= tantalum
CRT	= cathode-ray tube	LOG	= logarithmic taper			TD	= time delay
CW	= clockwise	LPF	= low pass filter	PH BRZ	= phosphor bronze	TGL	= toggle
				PHL	= phillips	THD	= thread
DEPC	= deposited carbon	M	= milli=10^{-3}	PIV	= peak inverse voltage	TI	= titanium
DR	= drive	MEG	= meg=10^6	PNP	= positive-negative-positive	TOL	= tolerance
		MET FLM	= metal film			TRIM	= trimmer
ELECT	= electrolytic	MET OX	= metallic oxide	P/O	= part of	TWT	= traveling wave tube
ENCAP	= encapsulated	MFR	= manufacturer	POLY	= polystyrene		
EXT	= external	MHZ	= mega hertz	PORC	= porcelain	U	= micro=10^{-6}
		MINAT	= miniature	POS	= position(s)		
F	= farads	MOM	= momentary	POT	= potentiometer	VAR	= variable
FH	= flat head	MOS	= metal oxide substrate	PP	= peak-to-peak	VDCW	= dc working volts
FIL H	= fillister head	MTG	= mounting	PT	= point		
FXD	= fixed	MY	= "mylar"	PWV	= peak working voltage	W/	= with
						W	= watts
G	= giga (10^9)	N	= nano (10^{-9})	RECT	= rectifier	WIV	= working inverse voltage
GE	= germanium	N/C	= normally closed	RF	= radio frequency		
GL	= glass	NE	= neon	RH	= round head or right hand	WW	= wirewound
GRD	= ground(ed)	NI PL	= nickel plate			W/O	= without

Table 5-2. Model 64223A 8018X Control Card Replaceable Parts

REFERENCE DESIGNATOR	HP PART NUMBER	CD	QTY	DESCRIPTION
A1	64223-66501	3	1	8018X EMUL CNTL - NEW
A1	64223-69501	9	1	8018X EMUL CNTL - EXCHANGE
MP1	1480-0116	8	2	PIN-GRV .062-IN-DIA .25-IN-LG STL
MP2	64223-85001	8	1	EXTRACTOR - "64223A"
MP3	64223-85002	9	1	EXTRACTOR - "EM8018X"
W1	64223-61601	4	2	CABLE - MEMORY INTERCONNECT

Table 5-3. Model 64224A 80186 Emulator Pod Replaceable Parts

REFERENCE DESIGNATOR	HP PART NUMBER	CD	QTY	DESCRIPTION
A1	64224-66501	4	1	80186 POD CPU BRD - NEW
A1	64224-69501	0	1	80186 POD CPU BRD - EXCHANGE
A2	64224-66502	5	1	80186 POD A/D BRD - NEW
A2	64224-69502	1	1	80186 POD A/D BRD - EXCHANGE
A3	64224-64101	6	1	COVER ASSEMBLY - BOTTOM
A4	64100-62102	4	1	ASSEMBLY - BRACKET GROUND
MP1	0400-0010	2	1	GROMMET-RND .25-IN-ID .375-IN-GRV-OD
MP2	0403-0179	0	4	BUMPER FOOT-ADH MTG
MP3	0520-0129	8	2	SCREW-MACH 2-56 .312-IN-LG PAN-HD-POZI
MP4	10230-62101	7	2	GRABBER ASSEMBLY
MP5	2200-0103	2	12	SCREW-MACH 4-40 .25-IN-LG PAN-HD-POZI
MP6	2200-0208	8	7	SCREW 4-40 0.750" LG
MP7	2200-0762	9	10	SCREW-MACH 4-40 .25-IN-LG TR-HD-POZI
MP8	5001-7080	9	1	CLAMP CABLE TOP
MP9	5001-7081	0	1	CLAMP CABLE BOTTOM
MP10	64224-04101	0	1	COVER - TOP
MP11	64224-94301	1	1	LABEL - 80186
MP12	64232-60201	9	2	ENDCAP ASSEMBLY
MP13	64224-00601	7	2	POD END SHIELD - RFI
MP14	7121-1780	0	1	LABEL - "HEWLETT-PACKARD"
MP15	7121-3182	0	1	LABEL - CABLE CAUTION
W1	64224-61802	8	1	CABLE - USER
W2	64224-61601	3	1	CABLE - POD BUS
W3	64242-61602	6	1	CABLE - USER ENHANCEMENT
W4	5061-1217	8	1	PROBE LEAD ASSEMBLY (WHITE/BLACK)
W5	5061-1218	9	1	PROBE LEAD ASSEMBLY (WHITE/BROWN)
A3	64224-64101	6	1	COVER ASSEMBLY - BOTTOM
A3MP1	64249-04102	0	1	COVER - BOTTOM
A3MP2	5001-0440	1	1	TRIM - SIDE
A3MP3	4040-1907	4	3	HEAT SINK - RUBBER
A3MP4	0470-1185	1	1	ADHESIVE - HEAT CONDUCTIVE

Table 5-3. Model 64224A 80186 Emulator Pod Replaceable Parts (Cont'd)

REFERENCE DESIGNATOR	HP PART NUMBER	CD	QTY	DESCRIPTION
A4	64100-62102	4	1	ASSEMBLY - BRACKET GROUND
A4MP1	1531-0273	7	1	MACHINED PART-SST BAR-CLAMP
A4MP2	2200-0151	0	2	SCREW-MACH 4-40 .75-IN-LG PAN-HD-POZI
A4MP3	2360-0117	6	2	SCREW-MACH 6-32 .375-IN-LG PAN-HD-POZI
A4MP4	2360-0129	0	1	SCREW-MACH 6-32 1-IN-LG PAN-HD-POZI
A4MP5	2420-0001	5	1	NUT-HEX-W/LKWR 6-32-THD .109-IN-THK
A4MP6	3050-0235	3	2	WASHER-FL MTLC NO. 4 .117-IN-ID
A4MP7	64100-01205	0	1	BRKT-GROUND

NOTES

Chapter 6
MANUAL CHANGES

This chapter normally contains information required to backdate the manual to earlier versions of the instrument. Since the manual applies directly to the only version of the Model 64224S existing, no backdating information is necessary.

NOTES

NOTES

Appendix A
SCHEMATICS

Appendix A contains schematics of the Model 64224A 80186 Emulator Pod for reference purposes.

NOTES
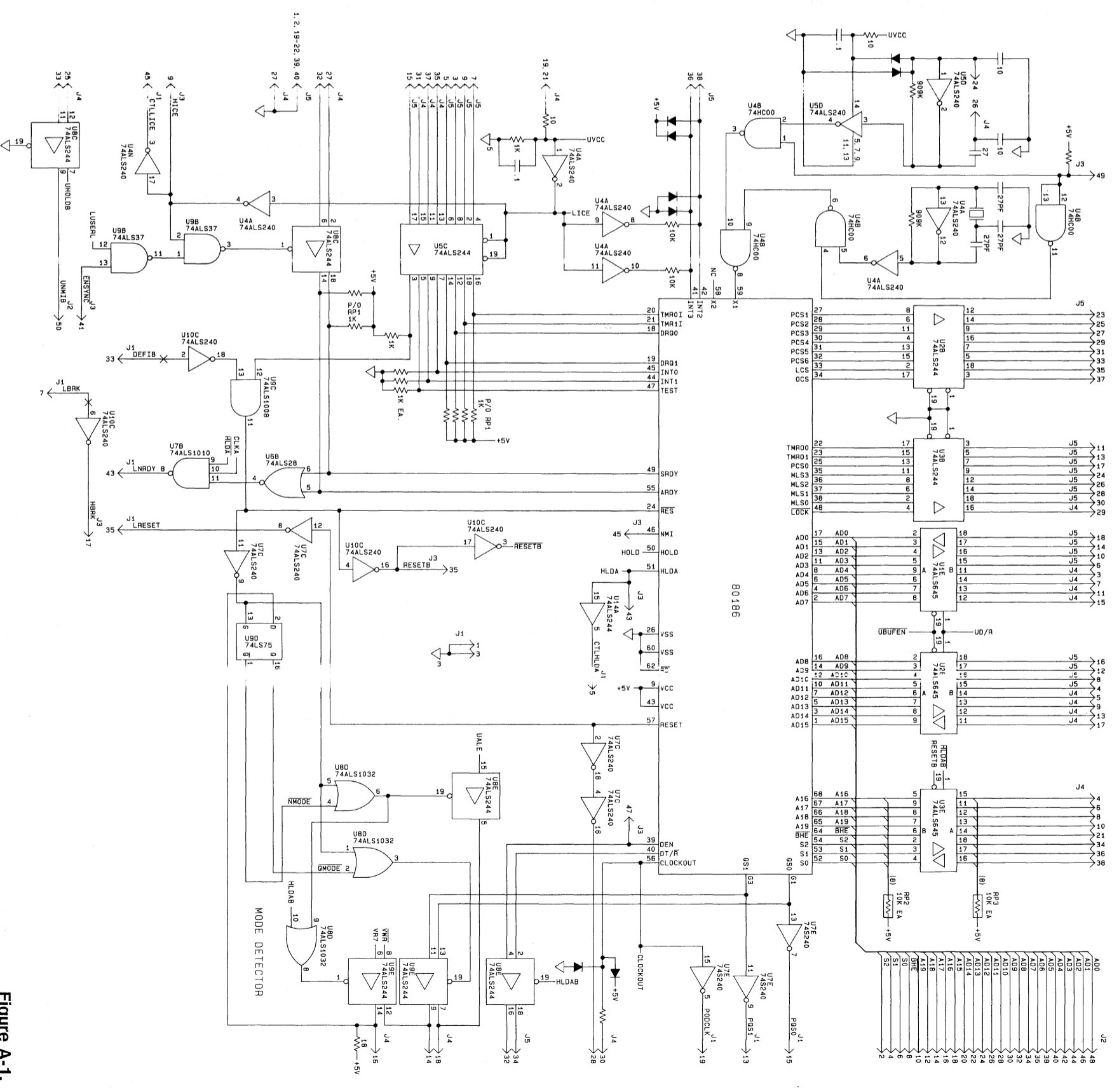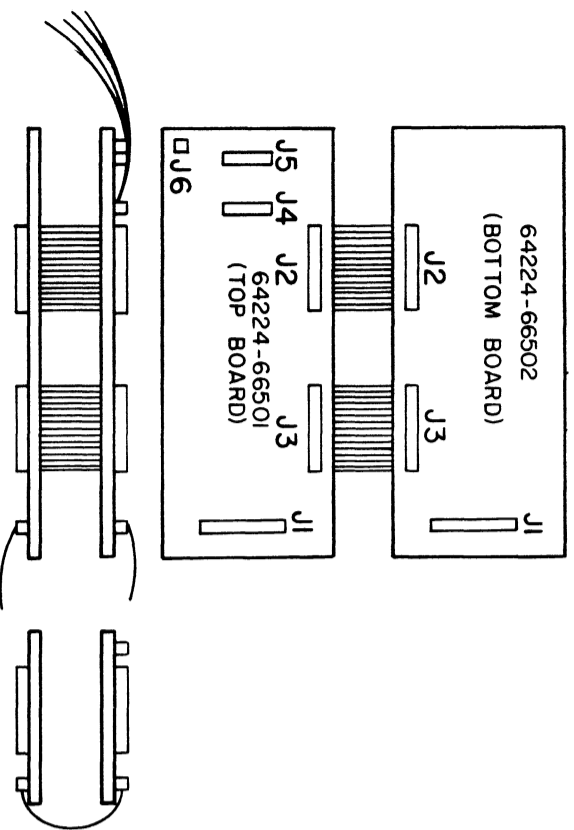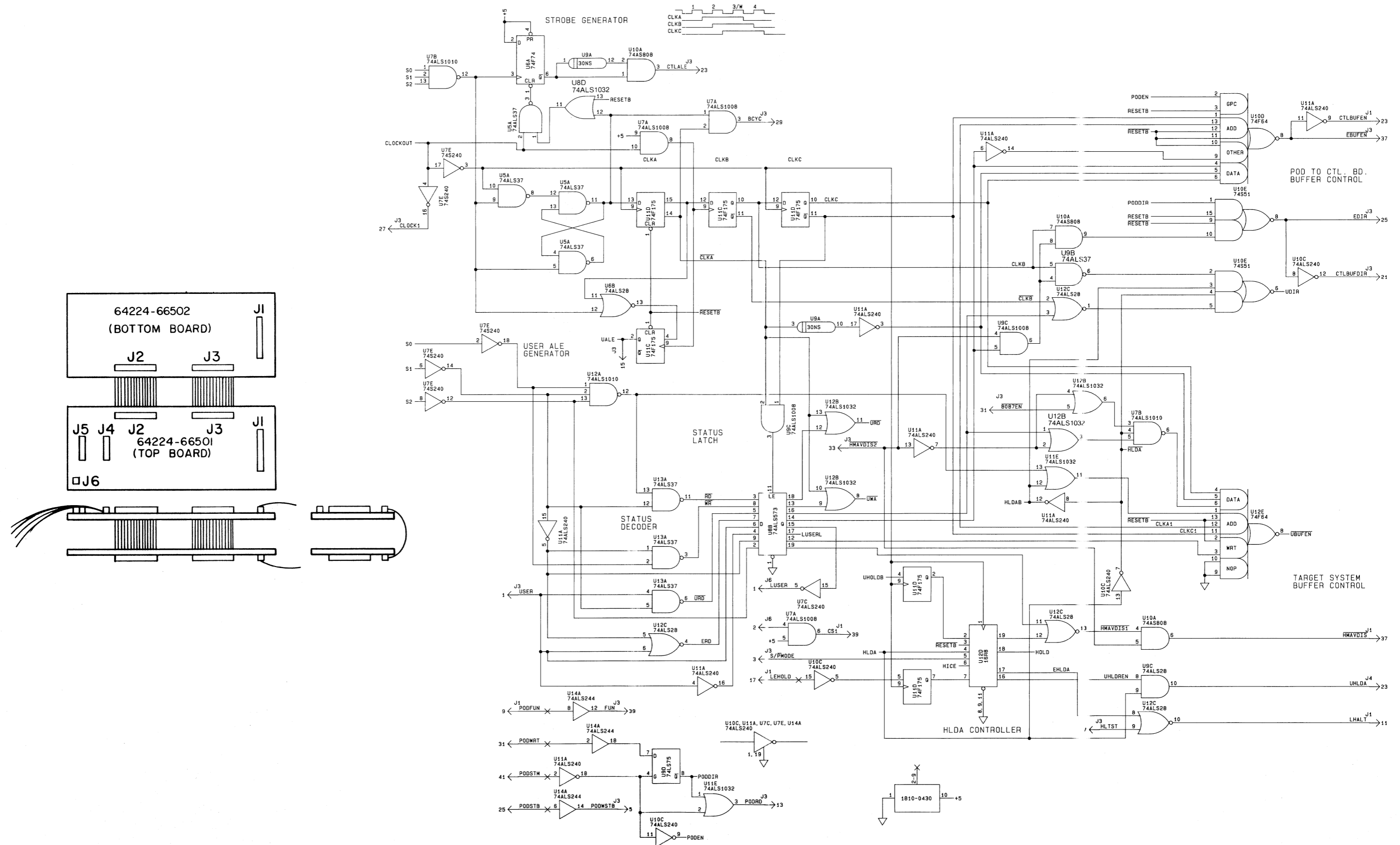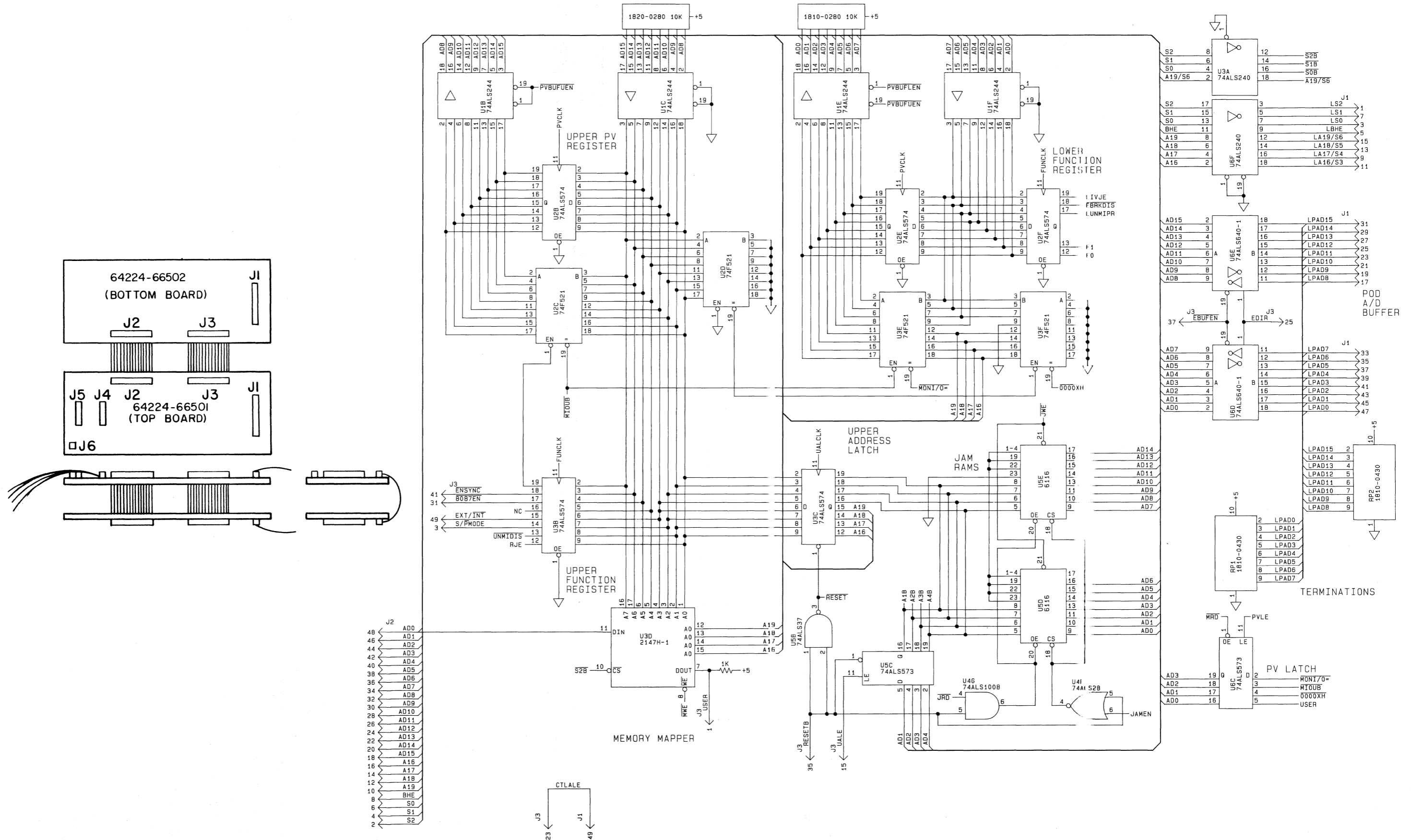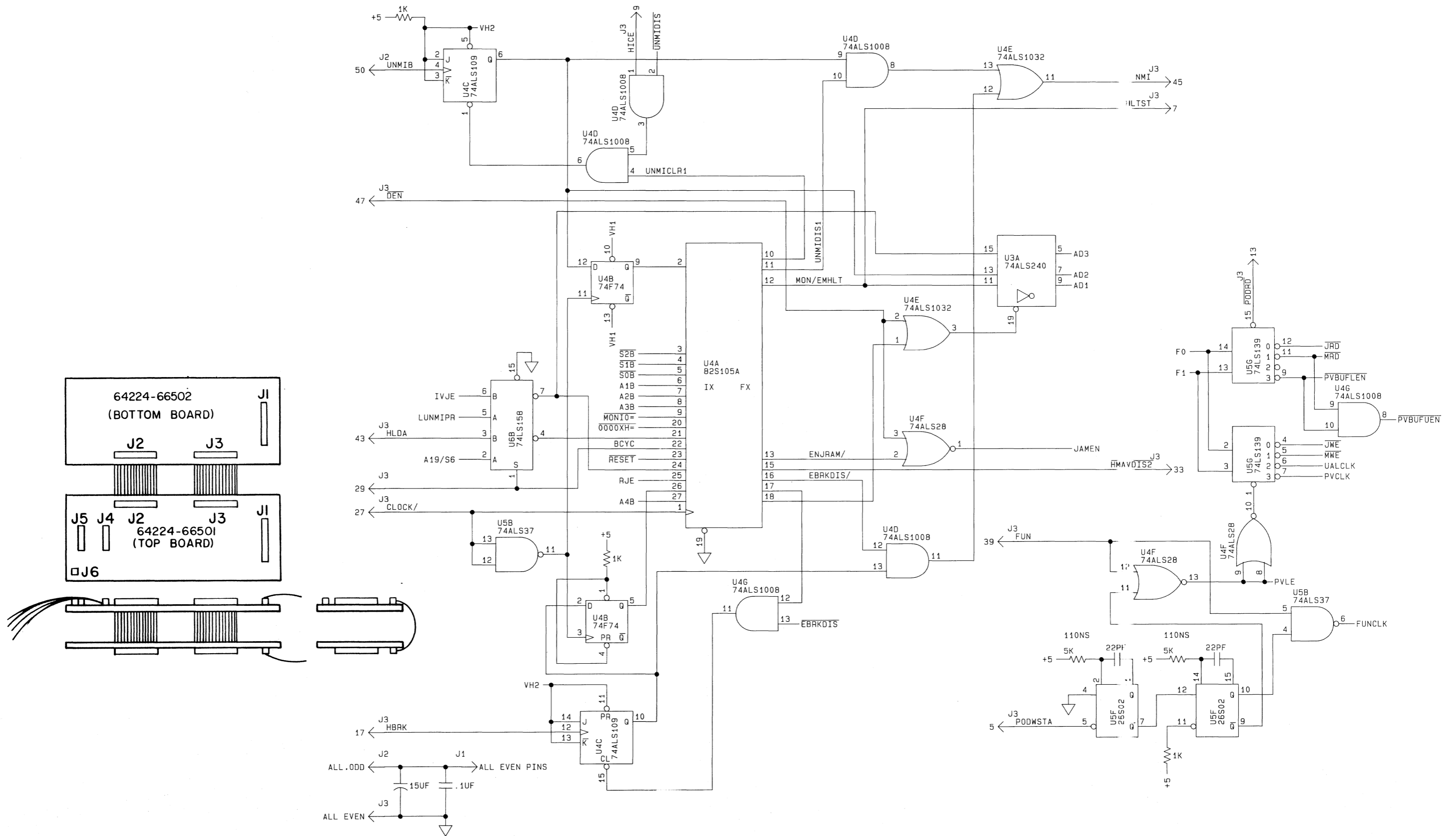
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Appendix B
SERVICE NOTES

SERVICE NOTES

This appendix contains all service notes which have been issued for the 80186 emulator up until the publication date of this manual. Table B-1 lists service notes contained in this appendix and the subjects that they cover.

Table B-1. Service Note Listing

Service Note   Subject

64223A-1   Anomalies caused by 80186 emulator in analysis performance verification.

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NOTES

64223A-1

S E R V I C E   N O T E

HP MODEL 64223A 8018X EMULATOR CONTROL CARD

All Serials

IMPROPER LANAL CIRCUIT

An anomaly has been identified with the LANAL analyzer clock line on the 80186 emulator. The emulator incorrectly leaves the LANAL line in the active state when it is not in use. As a result, analysis modules connected to the emulator will fail option_test performance verification. Also, analyzers which are not directly connected to the 80186 emulator analysis bus, but are connected via the IMB to an analyzer which is connected to the 80186 emulator, will fail the external IMB tests.

The solution is to remove the analysis bus cables which connect any analyzer to the 80186 emulator before running option_test performance verification on analysis modules in the cardcage.

The analysis bus cables must be reconnected before running the analysis stimulus tests from 80186 emulator performance verification. Otherwise, the emulator will not be able to communicate with the analyzer and the analysis stimulus tests will fail.

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HEWLETT PACKARD

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MANUAL IDENTIFICATION

> ### Manual Changes For All
> ### Emulator Pods And
> ### Preprocessors

This supplement contains important information for correcting manual errors and for adapting the manual to instruments containing improvements made after the printing of the manual.

To use this supplement:

Make all ERRATA corrections.

Make all appropriate serial number related changes indicated in the tables below.

Serial Prefix or Number	Make Manual Changes

Serial Prefix or Number	Make Manual Changes

▲ NEW ITEM

Your Hewlett-Packard emulator or preprocessor is marked with the international caution symbol shown below.

This symbol is included on each emulator and preprocessor because it is necessary for you to refer to your manual in order to protect against damage to the instrument. This symbol should appear in the table of contents of emulator and preprocessor manuals and on the pages that include cautions about installing the emulator or preprocessor probe into your target system. Caution statements are generally included in the Installation chapters, however, some manuals may not contain the appropriate caution statements. The appropriate caution statements for emulator pods and preprocessors are included here.

NOTE

Manual change supplements are revised as often as necessary to keep manuals as current and accurate as possible. Hewlett-Packard recommends that you periodically request the latest edition of this supplement. When requesting copies quote the manual identification information from your supplement, or the model number and print date from the title page of the manual.

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EMULATOR POD CAUTION

⚠

The following precautions should be taken while using Hewlett-Packard Emulator Pods. Damage to the emulator circuitry may result if these precautions are not observed.

POWER DOWN TARGET SYSTEM.

Turn off power to the target system and the emulation development station before inserting the user plug to avoid circuit damage resulting from voltage transients or mis-insertion of the user plug.

VERIFY USER PLUG ORIENTATION.

Make certain that Pin 1 of the target system microprocessor socket and Pin 1 of the user plug are properly aligned before inserting the user plug in the socket. Failure to do so may result in damage to the emulator circuitry.

PROTECT AGAINST STATIC DISCHARGE.

The emulator pod contains devices which are susceptible to damage by static discharge. Therefore, operators should take precautionary measures before handling the user plug to avoid emulator damage.

PREPROCESSOR CAUTION

⚠

The following precautions should be taken while using Hewlett-Packard State Analysis Preprocessors. Damage to the preprocessor circuitry may result if these precautions are not observed.

POWER DOWN SYSTEM UNDER TEST.

Turn off power to the system under test and the State Analysis system before inserting the user plug to avoid circuit damage resulting from voltage transients or mis-insertion of the user plug.

VERIFY USER PLUG ORIENTATION.

Make certain that Pin 1 of the target system microprocessor socket and Pin 1 of the preprocessor plug are properly aligned before connecting the preprocessor to the system under test. Failure to do so may result in damage to the preprocessor circuitry.

PROTECT AGAINST STATIC DISCHARGE.

The Preprocessor contains devices which are susceptible to damage by static discharge. Therefore, operators should take precautionary measures before handling the preprocessor plug to avoid damage to the preprocessor.

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